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Test & Measurement World

THE MAGAZINE FOR QUALITY IN ELECTRONICS

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TEST for the DIGITAL battlefield

Test Engineer of the Year John Gmitter manages a team charged with developing test stations that support Harris RF Communications' high-volume manufacturing of tactical communications equipment.

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MARCH 2007
VOL. 27 NO. 2

Test & MEASUREMENT WORLD®

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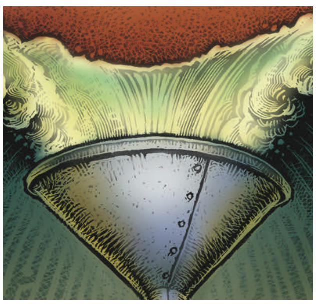

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Guest commentaries

Investment in JTAG standards development benefits entire industry

Glenn Woppman of ASSET InterTech says that active participation in formal standards work sanctioned by groups like IEEE, JEDEC, and PICMG can sometimes lead to the development of a standard, and so, too, can participation in ad hoc, informal working groups. The question of "formal vs. informal" doesn't really matter. The current status of the IJTAG and SJTAG activities offers a case in point.

65-nm IC designs need DWT as well as DFM

As process geometries shrink to 65 nm and below, manufacturing test must expand its role in the design, implementation, and production of semiconductor devices, says Sanjiv Taneja of Cadence Design Systems. Much like DFM and its manufacturing-driven design flow, which is an accepted requirement today, a "test-driven" design and implementation flow—which Taneja calls "design with test"—is now at the forefront of chip-design concerns.

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Reed Electronics Group

The Online Freedom Act returns

US legislators have a sorry record dealing with technology, as I commented previously on this page (September 2004) when I criticized the ill-conceived "Induce Act." But there are some situations in which legislative intervention might be beneficial, and one bill worth consideration is the "The Global Online Freedom Act of 2007," introduced by New Jersey Republican Rep. Chris Smith.

Smith first introduced his bill last year, following a Congressional hearing during which Internet company officials were criticized for contributing to Internet censorship. That bill died, but Smith is optimistic that the resubmitted version will

RICK NELSON, CHIEF EDITOR

win approval, in part because of emerging shareholder support for the measure. "Investors are taking notice of the repressive business practices…and are starting to voice their opposition," he said, adding that corporations need to "understand that it is good business to promote human rights."

The bill would prohibit US companies from disclosing information that personally identifies a particular user except for "legitimate foreign law enforcement purposes," and it would allow aggrieved individuals to file suit in any US district court.

A voluntary approach to online freedom is unlikely without a legislative threat.

Smith's bill has some problems. *New York Times* columnist Nicholas D. Kristof has written that its passage could drive US companies out of some countries, leaving their citizens with no alternatives to homegrown and heavy-handed Internet-restricting technologies. And Rebecca MacKinnon, a blogger and assistant professor at the University of Hong Kong's Journalism and Media Studies Centre, wrote earlier this year that the bill is "an overly blunt instrument" that promotes an "oversimplistic" good-country vs. bad-country world view.

The bill has some serious practical problems as well. How, for example, would a US company and foreign government agree on what constitutes "legitimate foreign law enforcement purposes" that would justify the company's disclosure of an individual's name? But I do agree with MacKinnon that the bill has helped to publicize the Internet censorship issue and has prompted shareholders and company management to focus on human-rights standards and practices.

MacKinnon advocates a nonconfrontational approach that might involve a voluntary global code of ethics for protecting privacy and freedom of expression. But at this point, I don't see that happening without the confrontational threat of a legislative blunt instrument. T&MW

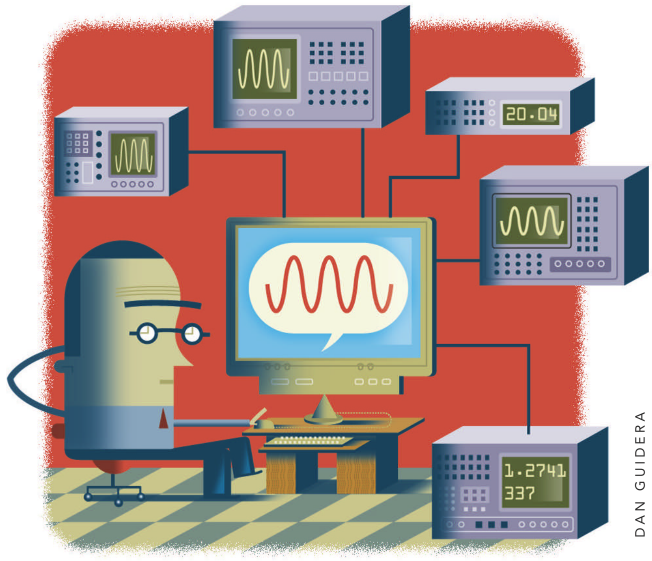
See the online version of this article for links to the text of the Online Freedom Act, to Kristof's and MacKinnon's writings, and to commentary from industry executives who testified at Smith's initial February 2006 hearing: www.tmworld.com/2007_03.

TESTVOICES

[An exclusive interview with a test engineer]

Share open-source test code

Mark Marlett is a principal design engineer at LSI Logic where he is the technical lead for SerDes devices. His responsibilities include design, specifications, and standards. Because LSI Logic manufactures custom ICs, the device under test (DUT) that Marlett deals with isn't the chip itself, but the SerDes intellectual property (IP) on the device. Test chips reside on a test board that contains a power supply, control logic (an FPGA), and connectors for DUT access. SerDes IP includes Fibre Channel, PCI Express, SerialATA, and Serial Attached SCSI. Marlett recently described his test processes to senior technical editor Martin Rowe.



DAN GUIDERA

Q: What tests do you perform on SerDes devices?
A: We start by making sure that the IP is functional. It must communicate with another device or with a bit-error-rate tester (BERT). We first must prove to the customer that a device works before we can stress it.

Once the chip is working, we program the SerDes receiver's adaptive-equalization filters for optimal values. At multigigabit data rates, the signals degrade to the point where there's no eye opening to measure. A typical IP has over 4000 possible filter settings. During a test, we measure BER, transmitter jitter, receiver jitter tolerance, and signal amplitude while we cycle through the DUT's states of operation. We measure these parameters over a range of temperatures and power-supply voltages.

Q: Do you automate your measurements?
A: We automate oscilloscopes, BERTs, and the DUT configuration. We use Python (www.python.org), an open-source scripting language.

Q: Why did you choose Python?
A: Python lets us write objects that represent the test equipment and the test chip. We can keep a test script to just a few lines because the control code is embedded in the object. We can, for example, change oscilloscopes and test chips without changing script code. IP designers give us a register map, and the test code reads the map to get the IP functionality. We're on the fourth generation of SerDes IP, all with the same test code.

We also use Python to perform signal analysis. By adding a math extension to the language, we have as much processing power as we'd get with a commercial data-analysis package—without buying a software license. We developed our own data-analysis objects. We compare our results to those we obtain using the analysis functions on the oscilloscopes. Because we use an open-source language, we can freely share test code with customers.

Q: How do the objects control the test chip?
A: The objects talk to the test board through a standard PC serial port. They control the power supply and send commands to the FPGA to control the test chips. We also have access to error codes on the test chips, and we use those codes to program the receiver equalizers. Thus, we can dynamically program the equalizers to open the receiver's eye diagram, although not in real time.

Q: How has automation improved productivity?
A: By creating Python objects, we minimize code duplication because engineers can often reuse working code with only small changes. Python code is self-documenting and is thus readable by both people and computers. That makes it easy for one engineer to use another engineer's code. T&MW

Every other month, we will publish an interview with an electronics engineer who has test, measurement, or inspection responsibilities. If you'd like to participate in a future column, contact Martin Rowe at mrowe@tmworld.com.

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USB Data Acquisition

Product Selection Chart

Category	USB Model	Summary	Analog Input Features				
			# of Channels	Throughput	Resolution (bits)	Input Range	A/D Type
Temp	DT9871 (Coming Soon)	48 thermocouple inputs, CJC per input, high accuracy, channel-to-channel isolation	48DI	10Hz per channel	24	± 1.250V (0.15µV LSB)	Delta-Sigma
Temp	DT9805, DT9806	7 thermocouples, 1 CJC, temperature applications, 500V isolation	8DI/16SE	50kHz**	16	±20mV, 100mV, 1V, 10V	SAR
Sound & Vibration	DT9837	4 IEPE (ICP) sensor inputs, tachometer, simultaneous A/Ds	4 IEPE (SE) + 1 Tacho	52.734kHz* per channel	24	±1V, 10V	Delta-Sigma
Sound & Vibration	DT9841-VIB	8 IEPE (ICP) sensor inputs, simultaneous A/Ds with DSP, 500V isolation	8 IEPE (SE)	100kHz* per channel	24	±10V	Delta-Sigma with DSP
Simultaneous High Speed	DT9832A	Simultaneous, 2 A/Ds @ 2.0MHz each, 500V isolation	2SE	2.0MHz* per channel	16	±10V	SAR
Simultaneous High Speed	DT9832	Simultaneous, 4 A/Ds @ 1.25MHz each, 500V isolation	4SE	1.25MHz* per channel	16	±10V	SAR
Simultaneous High Speed	DT9836	Simultaneous, up to 12 A/Ds @ 225kHz each, 500V isolation	6 or 12SE	225kHz* per channel	16	±5V, 10V	SAR
High Speed	DT9834	High-speed, up to 16 analog inputs, 500kHz, 16-bit, 500V isolation	16SE/8DI	500 kHz*	16	±1.25V, 2.5V, 5V, 10V	SAR
High Speed	DT9834-32	High-speed, up to 32 analog inputs, 500kHz, 16-bit, 500V isolation	32SE/16DI	500 kHz*	16	±1.25V, 2.5V, 5V, 10V	SAR
General Purpose	DT9801, DT9802	Multifunction analog I/O, 100 kHz, 12-bit, 500V isolation	16SE/8DI	100kHz**	12	0 to 1.25V, 2.5V, 5V, 10V; ±1.25V, 2.5V, 5V, 10V	SAR
General Purpose	DT9803, DT9804	Multifunction analog I/O, 100 kHz, 16-bit, 500V isolation	16SE/8DI	100kHz**	16	±1.25V, 2.5V, 5V, 10V	SAR
General Purpose	DT9821, DT9822	Simultaneous, highest accuracy, 24-bit, 500V isolation	4DI	960Hz per channel	24 variable	±39.0625mV, 78.125mV, 156.25mV, 312.5mV, 625mV, 1.25V, 2.5V (unipolar avail.)	Delta-Sigma
Low Cost	DT9810	Lowest cost, 10-bit, non-isolated	8SE	25kHz	10	0 to 2.44V	SAR
Low Cost	DT9812-2.5V	Low cost, 8 analog inputs, 12-bit, 2.5V range, non-isolated	8SE	50kHz	12	0 to 0.1525V, 0.305V, 0.61V, 1.22V, 2.44V	SAR
Low Cost	DT9812-10V, DT9813-10V, DT9814-10V	Low cost, up to 24 analog inputs, 12-bit, 10V range, non-isolated	8/16/24SE	50kHz	12	±1.25V, 2.5V, 5V, 10V	SAR
Low Cost	DT9816, DT9816-A	Low cost, simultaneous, 6 A/Ds @ up to 150kHz, 16-bit, non-isolated	6SE	50kHz/150kHz per channel	16	±5V, 10V	SAR
Low Cost	DT9853, DT9854 (Coming Soon)	Low cost, up to 8 analog outputs, 16-bit, 16 digital I/O, 1 C/T, 300V isolation	—	—	—		
Digital I/O	DT9817, DT9817-H	Low cost, 28 digital I/O, drives solid-state relays, non-isolated	—	—	—	—	—
Digital I/O	DT9817-R	Low cost,16 digital I/O, drives relays/motors, 500V isolation	—	—	—	—	—
Digital I/O	DT9835	96-Channel digital I/O, 500V isolation	—	—	—	—	—
DSP	DT9841, DT9841E	Simultaneous, 2 or 8 A/Ds @ 100kHz, DSP, 24-bit, 500V isolation	2 or 8DI	100kHz* per channel	24	±10V	Delta-Sigma with DSP
DSP	DT9842, DT9842/8	Simultaneous, 8 A/Ds @ 100kHz, DSP, 16-bit, 500V isolation	8SE	100kHz* per channel	16	±10V	SAR with DSP

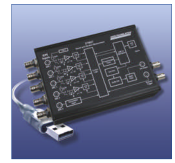
* *All functions synchronized for high speed: A/D, D/A, DIO, C/T, QD, Tacho* ** *Functions synchronized for A/D, DIO*

DT9816

DT9801

DT9834

DT9836



DT9837

DT9841

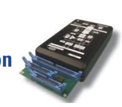
	Analog Output Features				Special Features							
	# of Channels	Throughput	Resolution (bits)	Output Range	Isolation	# of DIO	# of C/T	Quad Decoder	Tacho-meter	Power	Packaging	Starting Price
	—	—	—	—	600V Ch to Ch	8 in, 8 out	—	—	—	+5V	Thermo-couple Jacks	
	0 or 2	Single value	16	±10V	500V	8 in**, 8 out**	2	—	—	USB	STP	$985
	1	46.875kHz* Delta-Sigma	24	±10V	—	—	—	—	√*	USB	BNC/OEM	$1,445
	2	100kHz* Waveform	24	±2.5V, 10V	500V	16*	3*	—	√*	+5V	Sleek Box	$5,690
	0 or 2	500kHz* Waveform	16	±10V	500V	16 in*, 16 out*	2*	3*	√*	+5V	BNC/OEM	$1,970
	0 or 2	500kHz* Waveform	16	±10V	500V	16 in*, 16 out*	2*	3*	√*	+5V	BNC/OEM	$1,970
	0, 2, or 4	500kHz* Waveform	16	±10V	500V	16 in*, 16 out*	2*	3*	√*	+5V	BNC/OEM	$1,360
	0 or 4	500kHz* Waveform	16	±10V	500V	16 in*, 16 out*	5*	—	√*	+5V	BNC/OEM	$1,570
	—	—	—	—	500V	16 in*, 16 out*	5*	—	√*	+5V	STP/OEM	$1,850
	0 or 2	Single value	12	0 to 5V, 10V ±5V, 10V	500V	8 in**, 8 out**	2	—	—	USB	STP/EC	$675
	0 or 2	Single value	16	±10V	500V	8 in**, 8 out**	2	—	—	USB	STP/EC/BNC	$929
	0 or 2	Single value	16	±5V	500V	8 in, 8 out	—	—	—	USB	STP	$1,150
	—	—	—	—	—	20	1	—	—	USB	STP	$149
	2	50kHz	12	0 to 2.44V	—	8 in, 8 out	1	—	—	USB	STP	$229
	2	50kHz	12	±10V	—	4/8 in, 4/8 out	1	—	—	USB	STP	$299
	—	—	—	—	—	8 in, 8 out	1	—	—	USB	STP	$349
	4 or 8	Single value	16	±10V, 0-10V, 0-20mA	300V	16	1	—	—	USB	STP	
	—	—	—	—	—	28	1	—	—	USB	STP	$149
	—	—	—	—	500V	8 in, 8 out	1	—	—	USB	STP	$299
	—	—	—	—	500V	96	—	—	—	USB	STP	$725
	2	100kHz* per channel	24	±2.5V, 10V	500V	24*	3*	—	√*	+5V	Sleek Box/ OEM	$1,495
	2 or 8	100kHz* per channel	16	±10V	500V	24*	3*	—	√*	+5V	Sleek Box	$3,295

OEM Version

BNC Version

STP Version

EC Version



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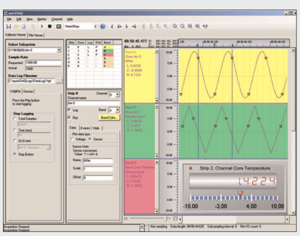
2 Ready-to-Measure Applications

quickDAQ



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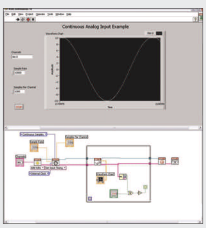
- Analyze data or save it to disk for later analysis
- Export data to other applications for advanced post-processing and analysis
- Converts signals automatically to engineering units to support applications ranging from temperature measurement to high-speed testing and analysis

3 Interface Software

LV-Link

(Interface to LabVIEW)

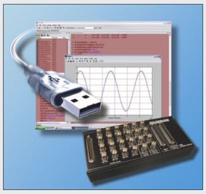


- Integrate DT and NI hardware in your program
- Stream to disk at full speed
- Get up and running quickly
- Use polymorphic VIs to speed development

4 DAQ Adaptor for MATLAB

(Interface to MATLAB)

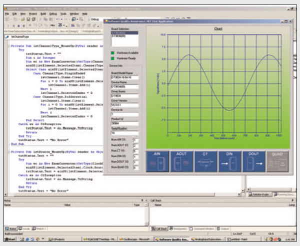
- Easy interface to all DT USB and PCI hardware



- Access live measured data directly from MATLAB.
- Supports analog input, analog output, and digital I/O capabilities
- Single environment for acquisition, analysis, and visualization

5 Low-Level Support

DT-Open Layers for .NET and DT-Display



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- Reduction of debug time through error detection and reporting
- Extensive example programs and documentation included
- Win32 SDK, C-DLLs
- .NET tools
- ActiveX controls
- DT-Display for easy data plotting

Aeroflex outlines strategy for 3G LTE test

During the 3GSM World Congress held February 12–15 in Barcelona, Spain, Aeroflex outlined its initial strategy for developing test products to support 3GPP's 3G LTE, which will involve the switch from W-CDMA to OFDM (orthogonal frequency division multiplexing) modulation technology. Aeroflex reported that it is designing the Aeroflex TM500 LTE and 6401 LTE to support the physical-layer testing of networks and mobile devices, respectively. A new graphical user interface will allow engineers to configure the LTE products without needing to write software to execute tests.

The TM500 and 6401 will also incorporate tools that will permit the generation of scripts needed to select the different configurations and tests. Scripts can be initiated by a test controller to synchronize control of the prototype under test and the test equipment. Users can alter parameters in real time to enable test coverage to be extended across a range of configurations used in a live system both in relation to test of the 3G LTE network and test of early 3G LTE prototype mobile devices. Aeroflex will develop test features especially for MIMO functionality to ensure that both the network and mobile devices are able to get the signaling right.

Because 3G LTE will coexist with UMTS systems based on W-CDMA and will integrate with GSM/GPRS/EDGE networks, Aeroflex reports that seamless handovers will be critical to the rollout of the first 3G LTE networks and the deployment of LTE mobile devices. The company said that the TM500 and 6401 will allow testing of these handovers—both at an early physical-layer-only test stage and then at the system test stage. www.aeroflex.com.

IEST announces new environmental testing certificate program

The Institute of Environmental Sciences and Technology (IEST) reports that it will unveil a new certificate program for advanced environmental testing during ESTECH 2007, its annual technical meeting. This year, ESTECH is scheduled for April 29 to May 2 in Bloomingdale, IL.

The certificate program will comprise four tutorials, each of which may also be taken as a stand-alone class: weather-encounter testing, pyroshock testing, multi-actuator testing and control, and shock analysis using the pseudo velocity shock spectrum. There will also be a separate tutorial on design characterization.

The pyroshock testing tutorial will cover the concepts of near-field and far-field pyroshock and their criteria. The multi-actuator testing and control tutorial will address spectral-density matrices, phase/coherence relationships, fixture design, and singularities in test equipment.

The tutorial on shock analysis will cover the shock spectra and the pseudo-velocity shock spectrum plotted on four coordinate paper (PVSS-4CP). The weather-encounter testing tutorial will discuss test facilities used for system verification, state-of-the-art high-speed diagnostics, and improved modeling and simulation approaches to predict hydrometeor demise across shocks and material impact response. www.iest.org/estech/estech.htm.

Editors' CHOICE

Tek recaptures scope bandwidth lead

Tektronix has reclaimed the real-time oscilloscope bandwidth lead with the DSA72004. This scope stretches its 16-GHz analog bandwidth to 20 GHz when you enable its DSP bandwidth enhancement. You can control the bandwidth between 16 GHz and 20 GHz, and the instrument can achieve full bandwidth simultaneously on all four channels.

A 20-GHz bandwidth lets you see the fifth harmonic of serial data streams at 12 Gbps and the third harmonic of signals at 8 Gbps. The ability to capture the fifth harmonic reduces the "dip" between the rising and falling edges, giving you more margin when making eye-mask tests.

The DSA7000 line also contains 16-GHz and 12.5-GHz models. All models have a maximum sample rate of 50 Gsamples/s, come with 200 Msamples of acquisition memory, capture up to 300,000 waveforms/s, and include software for analyzing serial data streams.

High-bandwidth scopes need high-bandwidth probes, and Tek has introduced the 16-GHz P7516 and the 13-GHz P7513 that let you switch among differential, single-ended, and common-mode measurements without changing probe setups.

Base prices: DSA72004—$158,000; DSA71604—$125,000; DSA712504—$99,500. P7516 probe—$14,500; P7513 probe—$11,000. *Tektronix, www.tektronix.com.*

Xantrex Technology to acquire Elgar Electronics

Burnaby, BC-based power-supply maker Xantrex Technology has announced that it entered into a definitive agreement to acquire Elgar Electronics of San Diego for $108 million (US). Elgar's product line includes AC-to-DC bench and system power supplies and AC-to-AC system power supplies, the latter coming from its acquisition of Sorensen in 1994. The company also manufactures electronic loads. www.xantrex.com.

NTS increases aerospace test capabilities

National Technical Systems has obtained a 90-kVA variable-frequency programmable power supply for its test laboratory in Fullerton, CA, to support RTCA/DO-160D/E, MIL-STD-704D/E, and ABD0100.1.8 (Airbus) test requirements. The ability to supply 400-Hz and 800-Hz power allows for increased testing frequency on aircraft components for Airbus and Boeing. Dwight Moore, COO of NTS, said that the company's Fullerton lab is one of the few US locations able to conduct this type of testing. www.ntscorp.com.

CALENDAR

International Reliability Physics Symposium, April 15–19, Phoenix, AZ. Sponsored by the IEEE. www.irps.org.

SAE World Congress, April 16–19, Detroit, MI. Sponsored by Society of Automotive Engineers. www.sae.org/congress.

International Microwave Symposium, June 3–8, Honolulu, HI. Sponsored by the IEEE. www.ims2007.org/.

To learn about other conferences, courses, and calls for papers, visit www.tmworld.com/events.

Editors' CHOICE

Reliability tester for power components

Intepro Systems' SEMTest configurable stress-screening system can perform accelerated lifetime testing of power semiconductors and modules incorporating IGBT, MOSFET, SCR, diode, and bipolar parts. The system can serve both manufacturers and users of power semiconductors who want to qualify commercial off-the shelf-devices for use in high-reliability applications found in automotive, aerospace, defense, industrial, and medical systems.

The core of SEMTest is a flexible architecture that can be modified to meet each customer's test requirements. Standard systems can be configured with from 20 to 1000 test cells; larger systems are available on special order. Each cell features its own local controller to set and monitor either applied or UUT power and other test parameters. Each cell also has a measurement unit for temperature, current, voltage, and timing, making it possible for complete characterization and production tests to accelerate failure mechanisms of individual devices and determine functional operating limits.

Capabilities include power cycling for thermal and electrical stressing, trend monitoring with user-defined control limits, rapid device temperature cycling and ambient temperature profiling, measurement of junction temperatures, and detection of nascent failures. Setups and measurements for each test cell are displayed on the screen and output into a SQL database for analysis.

Base price: $100,000. *Intepro Systems, www.inteproate.com.*

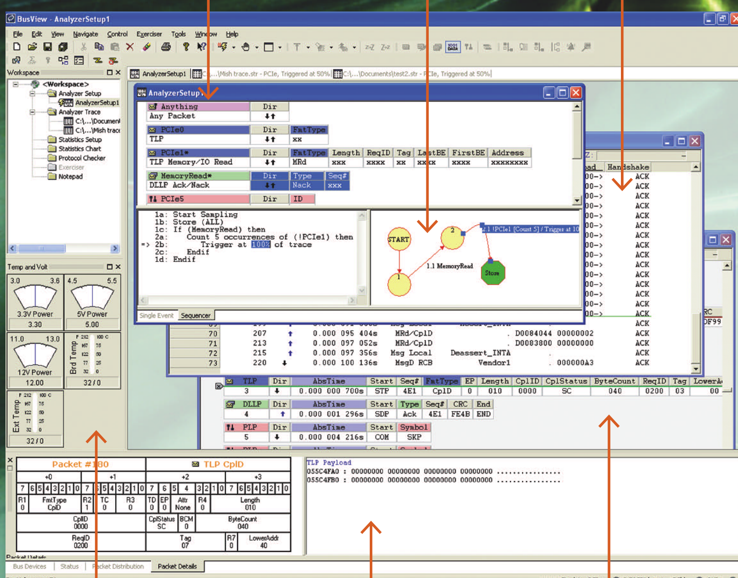
PCI Express made easy

with the Vanguard Express Analyzer

Packet based event trigger

Graphical sequencer

Data view



Voltage and Temperature monitor

Packet Details and Payload view

Packet based trace view

Powerful

- Supports x1 to x8 PCI Express
- Analyzer, Performance Monitor and Protocol Checker
- Search or Filter for an event or pattern quickly

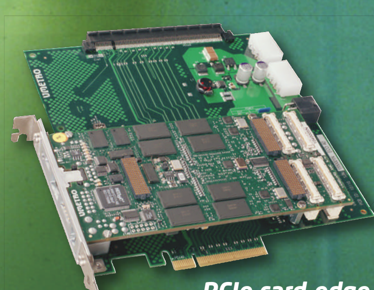
Flexible

- Ethernet or USB host connection
- All functions can operate concurrently and independently

Easy to Use

- Arrange trace data in Packet, Link, Split Transaction, Data or Lane Views with the click of a mouse
- Same GUI as the Vanguard PCI & VME analyzers
- Set up trigger events and sequences using drop down menus
- Extensive on-line help

XMC



PCIe card-edge

AdvancedMC

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VMETRO

innovation deployed

Measurement Science Conference expands exhibits

> > > Measurement Science Conference, January 21–25, 2007, Long Beach Convention Center, Long Beach, CA. www.msc.conf.com.

After a long run in Disneyland, the Measurement Science Conference moved to Long Beach, CA, for one year. Also for the first time, the MSC opened its exhibition hall on Wednesday, a day earlier than in previous years. In the past, the exhibits did not open until Thursday, and attendees who came for the NIST seminars on Monday and Tuesday and the workshops on Wednesday and then left would miss the Thursday and Friday technical session and exhibits.

"Exhibitors wanted to open the trade show a day early," said executive VP Kara Harmon. In commenting on the Wednesday opening, she added, "Exhibitors have seen a different clientele today."

MSC's main focus, the conference, ran Thursday and Friday. Andrew Willard, director of the International Bureau of Weights and Measures (BIPM), gave the keynote address and explained the BIPM's mission—worldwide measurement uniformity. "It all comes down to trade," Willard said to the audience. He explained how worldwide measurement traceability is important for trade but will take on more importance for measurements involving global warming. Willard also spoke of the need for improved chemical measurements to measure small amounts of drugs in the human bloodstream.

The MSC presented its annual Woodington Award to Dr. Howard Castrup of Integrated Sciences Group, Dave Deaver of Fluke, and Dr. Dennis Jackson of the US Navy's NSWC Corona, CA, facility. This marked the first time the Woodington award has been granted to three people. All were cited for their contributions to analytical metrology.

Dr. Howard Castrup, Dave Deaver, and Dr. Dennis Jackson (l-r) accepted the 2007 Woodington award for their contributions to analytical metrology.

Photo by Marie Roberts, courtesy of Measurement Science Conference.

Bob Fritzsche, president of MSC, presented the conference's first student achievement award to Shay Edwards, a high-school sophomore in California. Edwards received the award for his measurement work using an infrared thermometer to measure how a person's physical condition affects temperature transfer.

High school sophomore Shay Edwards received his student achievement award from Bob Fritzsche, president of the Measurement Science Conference.

Photo by Marie Roberts, courtesy of Measurement Science Conference.

Fritzsche told *T&MW*'s Martin Rowe about the large number of new faces at this year's conference. Fritzsche attributed that to engineers comings from Asia and from industries new to the conference. "We're seeing people from the medical industry coming here. ISO 17025 is also forcing people to come here to learn about measurement uncertainty." He estimated that about 40% of the attendees were new to MSC.

EXHIBITION FLOOR

This year's exhibition saw several new exhibitors. **Exfo** (www.exfo.com) appeared with its calibration system for optical instruments. Power-supply maker **Lambda** (www.lambdapower.com) also made its first MSC appearance with programmable power supplies. **Ohm Labs** (www.ohm-labs.com), a spinoff from Process Labs, exhibited a line of precision resistors used for calibrating resistance-temperature detectors (RTDs). The company also displayed precision shunts for high-current applications. New exhibitor **Rohde & Schwarz** (www.rohdeschwarz.com) exhibited RF signal sources used for calibrating spectrum analyzers.

New products are unusual in calibration, but a few did appear. **Fluke** (www.fluke.com), for example, added new products including a rubidium frequency reference and a waveform generator. The company showed its new resistance source for calibrating electrical safety (hipot) testers. T&MW

RICK NELSON
CHIEF EDITOR
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DigRF supports baseband and RF chipset test

DigRF (www.digrf.com) is emerging as a standard serial digital interface between 2.5G and 3G cell-phone baseband and RF chips. The standard has the support of RF IC, baseband IC, and cell-phone companies, and DigRF functionality is appearing on devices such as Freescale's RFX300-30 3G multiband RF subsystem, introduced last month.

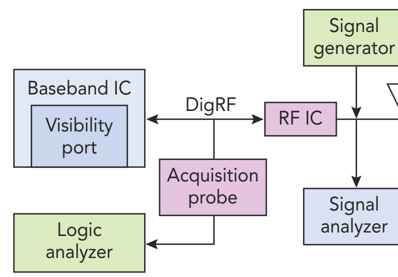
The standard specifies a 312-Mbps data rate and a choice of 1.8-V LVDS, 1.2-V LVDS, and SLVDS signal formats. One of DigRF's goals is to facilitate baseband and RF IC interoperability. DigRF consumes little power when operating (cell-phone designers can choose high-speed or low-power modes, depending on the needs of the product they are developing); it offers an even lower power sleep mode; it requires minimal real estate for interface circuits; and it uses as few as six conductors to link the baseband and RF chips. And, of course, it keeps cost to an absolute minimum.

In addition to providing those benefits, DigRF is serendipitously opening a window through which design and validation engineers can monitor data exchanges between baseband ICs and RF ICs. In fact, said Agilent product manager Jim Majewski, DigRF provides one of very few visibility points into cell-phone signals. (A baseband IC's visibility port provides another.)

To help take best advantage of that visibility, Agilent has introduced digital-acquisition and stimulus probes that make it easy to monitor DigRF traffic on a logic analyzer (see "Product Update," p. 61). The addition of a signal analyzer enables test of an RF IC's transmitter; a signal generator aids in the evaluation of its receiver (**figure**).

During RF IC validation, a stimulus probe can substitute for the baseband IC, which integrators might receive several months after getting their first RF ICs. Majewski noted that the probes and instruments can also be used to help fine-tune baseband algorithms to compensate for RF IC deficiencies—potentially avoiding costly re-spins. In addition to serving design and validation functions, the tools, he said, can also help manufacturing teams monitor lot-to-lot variations when the chips reach high-volume production.

I asked Majewski what would happen when the DigRF path itself is subsumed within a single chip integrating digital-baseband and RF circuitry. He said that for most phones he doesn't expect that to happen soon: "The two-chip approach has some legs." He acknowledged that a one-chip approach is attractive for very-low-cost cell phones. But he said that two-chip approaches provide more flexibility for adding features and that they are better equipped for supporting two-antenna schemes for optimizing signal quality, weeding out reflections, and minimizing dropped calls. T&MW



A DigRF acquisition probe enables a logic analyzer to monitor the DigRF serial bus; a baseband IC's visibility port enables correlation of internal baseband IC operations with DigRF traffic. A signal generator can help monitor receiver performance; a signal analyzer assists with transmitter measurements.

Faraday selects Verigy V93000

Verigy has announced that Faraday Technology, an ASIC and SOC design-service company, has selected the Verigy V93000 Pin Scale system for the test and validation of Faraday's SOC chipsets and IP portfolio. Faraday, the design-service partner to foundry UMC, adopted the Verigy system for IP/SOC design verification and test-program generation to foster mass production for its integrated device manufacturer (IDM), design-house, and system-house customers. www.faraday-tech.com, www.umc.com, www.verigy.com.

Parametric-parallel-test handbook

Keithley Instruments has published *Parallel Test Technology: The New Paradigm for Parametric Testing*, a 60-page handbook offering an overview of the emerging test technique known as parallel parametric testing, a strategy for wafer-level parametric testing that uses concurrent execution of multiple tests on multiple scribe-line test structures and helps semiconductor fabs maximize their test throughput and reduce their cost of test. The handbook is free. ggcomm.com/Keithley/PPTHandbook.html.

Alereon teams with Teradyne on RF test

Teradyne and Alereon have teamed up to use Teradyne's RF test technology to characterize the operational performance of Alereon's AL4000 family of ultra-wideband (UWB) devices. Teradyne's Flex RF ATE helped Alereon ramp up its production to deliver products to more than 50 customers in the second half of 2006. www.alereon.com, www.teradyne.com.

JON TITUS
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Vision Web sites fail to deliver

When I set out to write an article, I am able to contact knowledgeable people at OEMs who give me the latest information about technologies, trends, and ways to solve problems. Engineers who must design vision systems, however, rarely have this kind of access: They often must rely on company Web sites as they gather information. Unfortunately, many vendors take a simple flat-file approach and put only a gussied-up version of their catalog on line. That approach answers the "what with" question, but it leaves unanswered, "how to?"

I visited one vision company's site where I found a section that purports to help engineers find the right camera for an application. I entered specs for pixel resolution, interface type, and so on, which yielded 174 camera choices. A click on a camera's model number told me only whether the camera worked with the vision company's products. A click on the camera supplier's name led to a long "for more information" form, not to the camera company's Web site.

This 20Q electronic game can serve as a model when companies want their Web sites to deliver application answers, not just product specs.
Courtesy of Radica Games.

A lens vendor's Web site promises to provide information about lenses used in machine-vision applications. But click far enough down the menus and you'll find only a list of lens types, such as telecentric, zoom, variable mag, and micro-video, followed by specific lens data. Why would I need a telecentric lens instead of a micro-video lens? The site does not answer this fundamental question.

In each case, I had hoped for an interactive tool that would help me select products that would solve a specific inspection problem: Enter the dimensions of a product to inspect, its characteristics, required dimensional resolution, and so on, and a Web site would provide a list of possible cameras and links to manufacturers' sites. Or, enter a distance to a product, the required field of vision, resolution, and so on, and a Web site would offer lens choices.

Neither site mentioned above came close to acting like an advisor. Instead of helping engineers solve a problem, they simply list product specs.

As an example of a simple, yet useful, tool, check out the JavaScript security-camera lens calculator on the 2M Solutions Web site at www.2mcctv.com/lenscalculator.html. Users can enter any two of three characteristics—distance to target, lens size, or field of view—and the calculator computes the other.

The kids' game 20Q from Radica Games also serves as a good model for vendors and Web-site designers who aim to help engineers solve real problems. A player thinks of an object, and by asking the player 20 questions, the fist-sized electronic game homes in on the object's name. Players answer "yes," "no," or "sometimes" as the game poses a question such as, "Would you find it in an office?"

Three possible answers for each of 20 questions (sometimes a few more) could lead to over a trillion guessed objects, surely enough for vendors to home in on the specific answers engineers need to solve vision-application problems. You can beat the 20Q game with things such as "silicon and "gun powder," but most of the time this tiny brain wins. It's sad when a $13 game beats out most Web sites as a way to answer questions. T&MW

Dechow earns AIA achievement award

David Dechow, president of Aptúra Machine Vision Solutions, is the winner of the 2007 Automated Imaging Achievement Award. Dechow received the award from Automated Imaging Association executive director Jeffrey A. Burnstein on February 1 at the annual AIA Business Conference in Orlando, FL. "Mr. Dechow is being recognized for over 25 years of engineering and successfully implementing machine-vision solutions in a wide variety of industries," said Burnstein. www.machinevisiononline.org.

Cognex adds color offerings

Cognex has added color capabilities to its VisionPro PC vision software, including dedicated tools for color sorting, color identification, and color monitoring. "Cognex vision tools improve yield and productivity at many stages of production," said Kris Nelson, Cognex senior VP, Factory Automation. "Now, manufacturers can achieve similar gains in other applications where color inspection is required." www.cognex.com.

Halcon runs on Vista

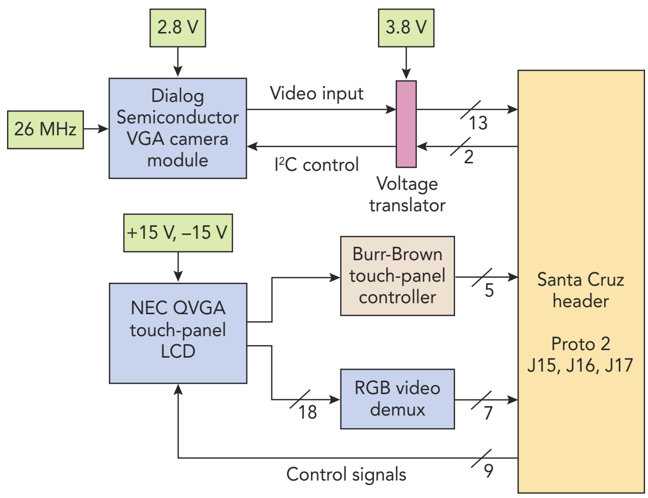
MVTec reports that release 7.1.2 of its Halcon machine-vision software library can run on Microsoft's Vista operating system. Halcon supports functions including blob analysis, morphology, pattern matching, metrology, 3-D calibration, and stereo vision. It also runs under Linux and Solaris. www.mvtec.com.

TEST EQUIPMENT DESIGN

FPGA designs for portable test gear

Traditionally, T&M OEMs have designed instruments to perform test procedures based on a specific standard, so they have been forced to redesign their products whenever a new or revised standard is published. Now, vendors are looking to make their communications testers, semiconductor ATE, and general-purpose test instruments more flexible so they can adapt to changing specifications. At the same time, customers are looking for test equipment that is more portable to increase productivity and reduce capital expenses.

Field-programmable gate arrays (FPGAs) may provide the answer to both needs. FPGAs continue to make inroads into the growing universe of portable gear. A single FPGA design can support many feature sets, and FPGA-based portable test gear is field-upgradeable to accommodate new test standards. An FPGA can implement the functionality of portable-test-device components such as CPUs, display drivers, keypad interfaces, and generic I/O ports. Specific designs can augment common functions with unique elements such as digital-signal processing (DSP) blocks. Reprogramming an FPGA takes care of required variations in functions such as display size and resolution and number of keys.



The portable reference platform (PRP) comprises a software processor development board, display touch-panel board, and VGA video-output board.

A good starting point is a portable reference platform (PRP) from an FPGA vendor (**figure**). Such a platform helps you evaluate software productivity tools, embedded processors, and system-on-a-programmable-chip (SoPC) design tools for embedding LCD, touch-panel, and CMOS imaging IP cores in an FPGA. Also, IP blocks such as hardware acceleration and image edge detection are included to give designers an understanding of the FPGA's DSP and coprocessing capabilities.

The online continuation of this article at www.tmworld.com/2007_03 includes design metrics related to the PRP, recommendations for preserving software investments, and an application example involving automotive noise, vibration, and harshness (NVH) test.

Charlie Jenkins, Altera

DATA TRANSFER

What does GT/s mean, anyway?

When announcing version 2.0 of the PCI Express (PCIe) standard in January, the PCI Special Interest Group (PCI-SIG) said that the new version "doubles the interconnect bit rate from 2.5 GT/s to 5 GT/s." Most of us are used to seeing bus speeds specified in Gbps, or gigabits per second, but GT/s stands for gigatransfers per second. What's the difference?

The difference has to do with the encoding of the data. Because PCIe is a serial bus with the clock embedded in the data, it needs to ensure that enough level transitions (1 to 0 and 0 to 1) occur for a receiver to recover the clock. To increase level transitions, PCIe uses "8b/10b" encoding, where every eight bits are encoded into a 10-bit symbol that is then decoded at the receiver. Thus, the bus needs to transfer 10 bits to send 8 bits of encoded data.

Looking at a single PCIe 1.1 lane, the bidirectional bus can transfer 2.5 Gbps in each direction, or 5 Gbps in total. Because the bus needs to send 10 bits of encoded data for every 8 bits of unencoded data, the effective bit rate is

$$5 \text{ Gbps} \cdot (8/10), \text{ or } 4 \text{ Gbps}$$

A 16-lane PCIe 1.1 bus can transfer 80 Gbps of encoded data or 64 Gbps of unencoded data. Because PCIe 2.0 doubles the transfer rate, a single lane can transfer 5 Gbps of unencoded data in each direction, or 10 Gbps of unencoded data in total. That's 8 Gbps encoded. Thus, a 16-lane PCIe 2.0 bus transfers 160 Gbps unencoded, which is 128 Gbps of encoded data. That's 16 Gbytes/s of encoded data.

So, when the PCI-SIG announced the new rate of 5 GT/s, it was referring to raw data rate—the number of bps that the bus can move, or transfer. The encoding process reduces the rate of useful data transferred over the bus to 80% of the bus's raw speed.

See the online version of this article for links to more about PCI Express, data encoding, and transfer rates. www.tmworld.com/2007_03.

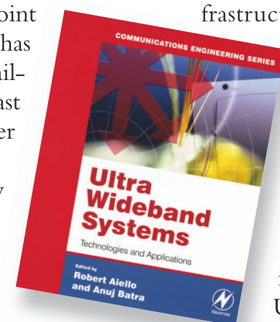
Martin Rowe, Senior Technical Editor

BOOK REVIEW

Do we have a failure to communicate?

Ultra Wideband Systems: Technologies and Applications, edited by Robert Aiello and Anuj Batra, Newnes, 2006. 323 pages. $69.95.

Ultra wideband (UWB) technology has taken more than 45 years to get to the point where it's at today—to the point where Maury Wright, chief editor of *EDN*, says "I hope the UWB crowd either finally delivers products in 2007 or just disappears." Wright's point is well taken, as UWB has thus far demonstrated a failure to communicate, at least in high-volume consumer applications.



But the technology holds significant promise for applications such as wireless USB, which, as Robert Aiello points out in the concluding chapter of *Ultra Wideband Systems*, can readily make use of UWB's high-bit-rate, short-range communications capabilities. Beyond cable-replacement chores, Aiello says UWB can also serve applications such as digital cameras and portable media players, for which no cable alternatives exist.

But the bulk of *Ultra Wideband Systems* deals with UWB technology, not applications. And given that the applications will emerge, this book provides a good overview of what UWB is and how it works.

For most of UWB's history, it served in the military and in labs, with the term "ultra wideband" itself appearing in the late 1980s, apparently from the Department of Defense, according to Aiello. The more consumer-centric version was born on Valentine's Day 2002, former FCC chief engineer Edmond J. Thomas reports in a forward to the book, when the FCC issued a necessary approval despite complaints that UWB would occupy 7.5 GHz (3.1 to 10.6 GHz) of already-licensed spectrum.

The book introduces UWB technology, beginning with Shannon's theorem: $C = W\log_2(1 + S/N)$, which demonstrates that it is more effective to increase bandwidth, W, which is linearly related to capacity, C, than to increase power, S/N, which is logarithmically related.

The second chapter discusses regulatory requirements and the governing organizations as well as the testing infrastructure, focusing on anechoic chambers, open-area test sites (OATS), and alternative environments such as mode-tuned or mode-stirred chambers. As for instrumentation, chapter author Robert Sutton notes that time-domain instruments used for UWB measurements require large instantaneous bandwidths, while frequency-domain measurements can be made with instruments having limited bandwidths if properly staged.

Chapter 2 is the only one that focuses extensively on test, but the entire book could be said to deal with measurement in that it describes the parameters and characteristics you have to verify if you find yourself developing UWB products. Other chapters cover interference, UWB antennas, direct-sequence and multiband (including multiband OFDM) UWB approaches, and UWB MAC design. In one chapter, Naiel Askar, Susan Lin, and David Furuno of General Atomics describe the Spectral Keying UWB modulation scheme developed by their company; the advantage, they write, is the technique's scalability.

It remains to be seen which techniques will be essential to UWB's success as developers "focus on simplifying use, streamlining costs, and staying ahead of advancing data rates," according to Aiello. This book serves as a good foundation on which developers can build. (Note: The publisher is owned by *Test & Measurement World*'s parent company.)

Rick Nelson, Chief Editor

Get Higher ATE Throughput – at Lower Costs

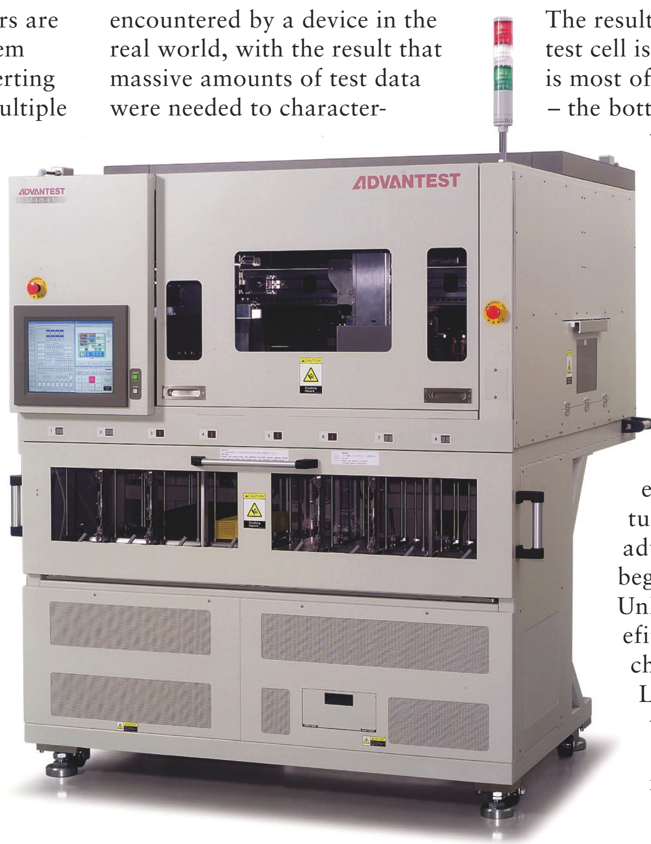
Despite the proliferation of BIST and DFT techniques, the handler is now the critical element in testing success.

The language in cars ads for fuel economy warns consumers, "Your mileage may vary." A similar caveat should be applied when engineers consider testing throughput. If you are still looking just at the published throughputs for your ATE gear, you are in for a rude awakening. Those figures provide only one clue to overall performance in actual use.

To be sure, several developments are improving ATE throughput. For example, test productivity in commodity memories has advanced quickly through increasing parallelism. Next generation memory testers are expected to offer the capacity of testing more than 1,000 devices per test cell – twice the parallel test capacity of the previous generation. Equipment manufacturers are increasing parallelism in System on a Chip (SoC) test by converting single-site test programs to multiple devices under test, multi-site test programs.

On another front, also in SoC test, the industry is moving toward an open architecture approach that can provide further improvements in throughput by enabling best-in-class instruments from different vendors to be combined and upgraded. A case in point: the Semiconductor Test Consortium and its OPENSTAR® architecture specification, which calls for a new, multi-site distributed-tester architecture.

Within devices, too, there's been tremendous progress. Design for Test (DFT) and Built in Self Test (BIST) are reducing testing cycles and test costs for complex mixed signal and digital semiconductor devices. Previous generations of testers were required to duplicate all the conditions that could be encountered by a device in the real world, with the result that massive amounts of test data were needed to characterize a complex SoC. Today, in many cases test can be accomplished much more quickly taking advantage of a device's BIST and DFT capabilities. This substantially reduces the amount of data that must be pumped into and out of the device under test.



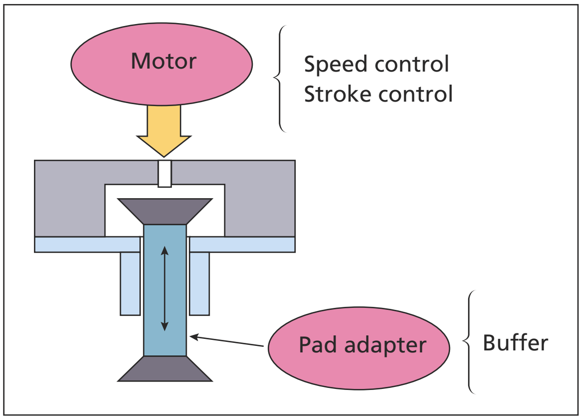
Advantest's M4841 doubles the capacity of earlier handlers, delivering high throughput of up to 18,500 devices per hour.

The Hidden Challenge

However, while the proliferation of BIST and DFT techniques in integrated circuits (ICs) is driving reductions in test times, the time required to actually index ICs in the tester often remains unchanged. The result is that when the entire test cell is considered, the handler is most often the defining element – the bottleneck – that determines the throughput. In other words, the most effective way to reduce the overall cost of testing is to improve the performance of the handler.

But that's not a trivial task. Newer packages can easily be damaged by picking and socket-plunging, and even by the forces experienced in a fast, tight turn. Fortunately, recent advances in handlers have begun to make a difference. Unlike the tester, which benefits from the better-faster-cheaper mantra of Moore's Law, the handler is subject to the limitations of Newtonian physics. Simply increasing the speed isn't difficult per se. However, increasing the speed – getting more ICs into and out of ATE sockets more quickly – is challenging if you intend to do so without jamming the handler, causing downtime, or damaging the chips, affecting yields. Some innovations that address these issues are computer simulation to optimize the speed at which devices can be moved and sophisticated optical alignment techniques that now help avoid jams and pin damage.

The latest generation of handlers has improved the speed with which devices can be moved from tray to socket and socket back to tray while avoiding jams and damage to delicate devices. A good example of this innovation is Advantest's M4841, a recently introduced handler that doubles the capacity of earlier handlers. It is capable of parallel tests of up to 16 devices and delivers high throughput of up to 18,500 devices per hour at a test time of three seconds or less.



"Soft touch" functionality, found in the M4841 handler, allows operators to adjust the amount of pressure to the device being handled, avoiding damage to tiny, light-weight devices that can't stand as much pressure as larger packages

On the leading edge

These new handlers also feature an innovative electro-pneumatic air pressure control system that makes it possible to set the contact pressure on the package precisely by software. This new "soft touch" functionality allows operators to adjust the amount of pressure to the device being handled, avoiding damage to tiny, light-weight devices that can't stand as much pressure as larger packages.

Among other new technologies now found in the latest handlers are vision alignment systems that provide feedback to continually improve positioning accuracy. This is particularly essentially, given the less than 0.5 mm width, fine-pitch devices now being employed in high-density IC packages, (including chip-scale and quad-flat packages and ball-grid arrays). In fact, alignment accuracies two times better than traditional mechanical alignment equipment can be maintained to 4 sigma levels.

Incorporating optical technology, Advantest's M4741A dynamic handler uses state-of-the-art vision alignment for precise positioning of fine-pitch (<0.5 mm) devices. This optical alignment process can achieve a 99.9% contact yield, which is particularly valuable when testing high pin count devices. Indeed, throughput can exceed 4,000 units per hour when performing simultaneous testing of four devices. This performance ensures rapid time to market for these advanced device packages, which are essential to cell phones, PDAs, notebook computers and other consumer products that require highly miniaturized, power-efficient semiconductors.

So, as manufacturers push to trim test costs, the most promising area for future improvements is clearly with the handler. Technological gains here have the potential to substantially boost overall performance, which should lead to a significant reduction in the cost of test. ■

How to Calculate ATE Cost and Performance

As the average selling price of semiconductors falls, manufacturers continue their campaign to curb test costs. You can calculate the Cost of Ownership of a test cell over its lifecycle as the sum of capital expenditures plus operating expenditures plus yield loss divided by throughput.

To calculate throughput: Multiply the good units you test per hour times the utilization times the uptime of the equipment. Capital expenses can then be calculated by adding the base price of the equipment plus any upgrades and peripherals and dividing by the economic life of the equipment. When you calculate operating expenses, in addition to the operators of the machine, make sure to also consider the time demands of the engineers and technicians who support your testing programs.

FOR MORE INFORMATION

Engineers can learn more about Advantest Corporation, the global leader in automatic test equipment for the semiconductor industry, by visiting www.advantest.com.
For more on the new M4841 Dynamic Test Handler, visit:
http://www.advantest.co.jp/products/ate/M4841/en-index.shtml

FIBER-OPTIC TEST

It's all in the alignment

DEVICE UNDER TEST
Fiber-optic waveguide modulators used in communications networks. The modulators, which often require special connectors, work in conjunction with polarization-maintaining (PM) fibers, mostly Panda fibers.

THE CHALLENGE
Replace standard angled physical contact (APC) fiber-optic connectors with those specified by customers, typically physical-contact (PC) connectors. Properly align the replacement connector for maximum on/off ratio.

THE TOOLS
- Agilent Technologies: optical power meter. www.tm.agilent.com.
- Lightel Technologies: polarization-maintaining laser light source. www.lighteltech.com.
- Tektronix: function generator. www.tektronix.com.

PROJECT DESCRIPTION
Lightel Technologies (Kent, WA; www.lighteltech.com) manufactures fiber-optic components that use polarization-maintaining (PM) fibers and PM connector terminations. The company typically uses angled physical contact (APC) connectors, but because some applications require waveguide modulators with physical contact (PC) connectors, customers often send their modulators to Lightel for a replacement connector.

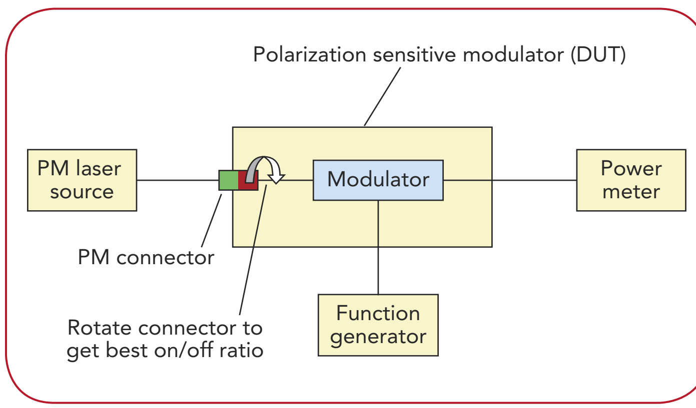
Although each modulator's polarization is aligned and optimized at the factory, cutting off and replacing the connector requires new polarization alignment. Therefore, operators who replace a connector must properly align the new connector to the fiber's polarization plane to maximize the fiber's on/off power ratio.

Fiber-optic connectors have alignment keys, and Lightel's operators visually align the polarization axis of the PM fiber to the key. Known as Panda fibers, the PM fibers look like the face of a panda when viewed as a cross section (Ref. 1, 2).

The alignment key provides a passive visual alignment, but there's still room for error. To optimize on/off ratio, operators apply power to the modulator and rotate the connector about 1° to 2° while monitoring its output. This active alignment improves the ratio from 15 dB to 25 dB.

An automated system (**figure**) produces PM light, controls the modulation, and measures output power swing at the connector. Operators use the power meter's min/max measurements to monitor the on/off ratio while they manually align the connectors to the fiber.

A PM laser light source produces light for the modulator, and a function generator produces the modulating signal—a 10-Hz sine wave. Operators rotate the connector and look for the largest on/off ratio, which occurs when the modulator's transfer function is at its peak as opposed to its trough.



A power meter measures optical power while an operator aligns a modulator's connector to its fiber.

LESSONS LEARNED
"A sine wave provides continuous modulation voltage so the power meter can catch all possible modulator output levels," said Shyh-Chung Lin, Lightel's VP of business development. "We match the frequency of the modulation signal to best match the sample rate of the power meter.

"The power meter takes 10 ms to 20 ms per sample, so the operator must wait until the meter samples the maximum and minimum light levels. When alignment is achieved, the operator glues the connector to the fiber. An alignment takes about 30 min."

Lin added, "Active alignment and in-situ monitoring is crucial to achieve the best performance in PM fiber with a waveguide modulator. With some engineering creativity, we were able tackle this measurement challenge using common test equipment."

Martin Rowe, Senior Technical Editor

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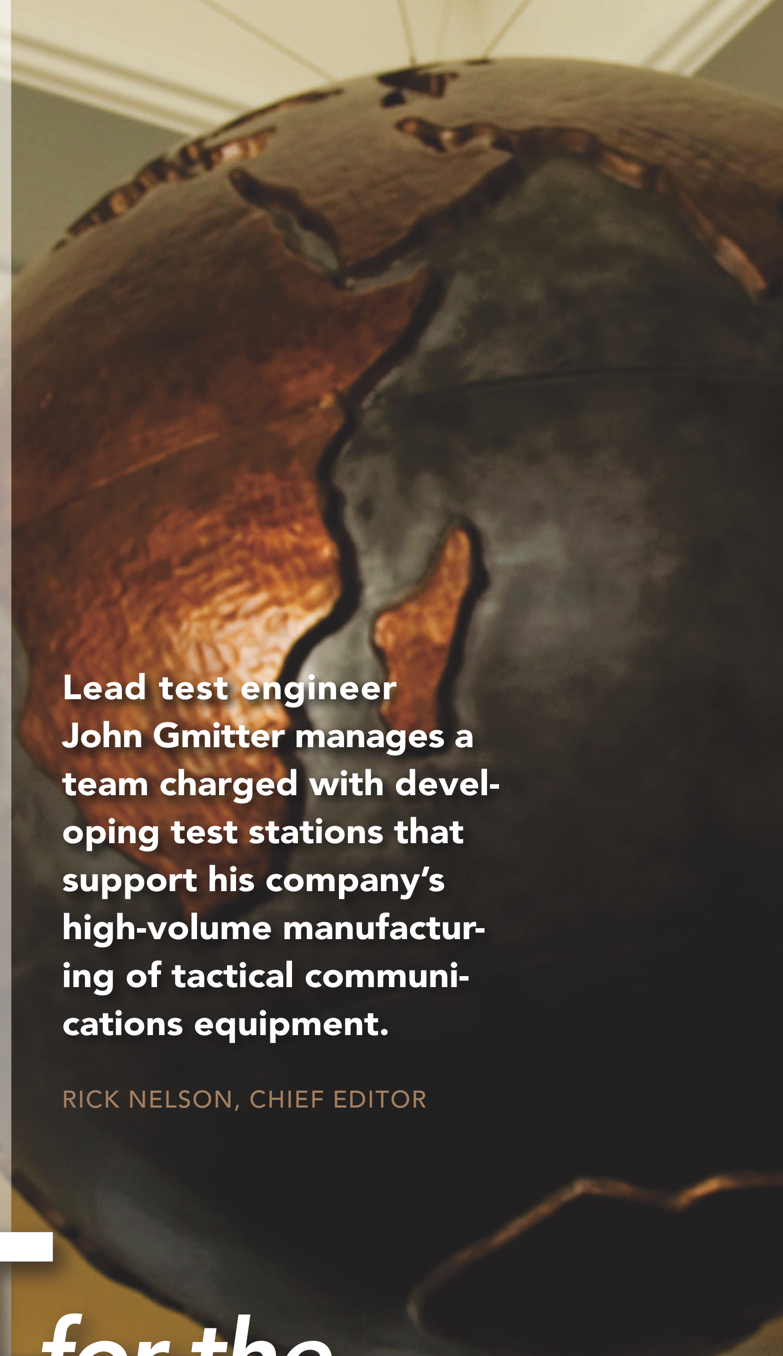


TEST *for the* DIGITAL battlefield

Lead test engineer John Gmitter manages a team charged with developing test stations that support his company's high-volume manufacturing of tactical communications equipment.

RICK NELSON, CHIEF EDITOR

ROCHESTER, NY—Team sports are a natural fit for Test Engineer of the Year John Gmitter, whose college baseball program competed with his engineering course work as he earned his first college degree. His teamwork skills serve him well at Harris RF Communications, where he was charged with taking control of a diverse group of engineers to upgrade Harris's test capabilities to keep up with ever-increasing production volumes for the company's products.

Those products include the Falcon II series of complete tactical vehicular, base-station, and handheld communications systems. Combined with the Harris RF-6010 Tactical Network Access Hub, the radios form the basis of the Harris Tactical Network, which speeds critical voice, data, and position information to and from the digital

In our September 2006 issue, we profiled the accomplishments of six outstanding test engineers from various industries, and we asked our readers to vote for the Test Engineer of the Year. Your choice? John Gmitter of Harris RF Communications.

As part of his award, John has designated Monroe Community College to receive a $30,000 engineering grant, courtesy of award sponsors Agilent Technologies, Keithley Instruments, and National Instruments.

FOREST MCMULLIN

battlefield, allowing radio operators to send and receive phone calls and enabling radio outstations to have wireless IP connectivity.

Navy experience

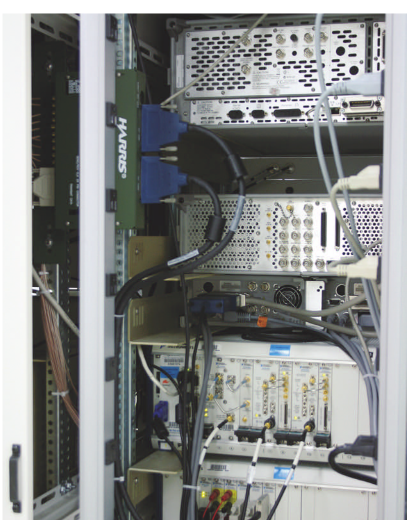
It was his experience with Harris communications products as an aviation technician in the US Navy that led Gmitter to seek employment with the company. He served in the Navy for four years, he said, where his duties included working on F-14 Tomcats onboard the USS Constellation.

"In my last deployment in the Navy," Gmitter explained, "I was troubleshooting a station that we used to test the black boxes in the planes, and I had to call Harris customer support"—his first contact with the company. When the Rochester native left the Navy in 1999, it seemed natural to him to apply to Harris.

As for the Navy service itself, that also came naturally: "My father and my father's father were both in the Navy, and I had heard lots of stories about military life." On obtaining his degree in electrical engineering, he was drawn toward enlisting. "I figured, if I don't do it now, I will never do it. And it was a fantastic, outstanding experience. It was hard work, but I really enjoyed it."

Before joining the Navy, Gmitter earned two degrees. A long-time interest in technology prompted him to take engineering courses at Monroe Community College, but that's one time where his teamwork got him into trouble. "One of my profs told me right when I signed up for his class, 'Oh, you're a baseball player. If you go on the spring trip, you will fail my class, I guarantee it.'"

Test Engineer of the Year John Gmitter deploys a production test station at Harris RF Communications' new Carlson Road facility. Courtesy of Harris RF Communications.



The Harris NPI test team based its test-station architecture on the PXI platform, which offers sufficient flexibility to accommodate other types of instruments. Courtesy of Harris RF Communications.

Gmitter was unconvinced. "I said to myself, that really doesn't sound right—I think I can handle it. So, I went with the team on the spring trip and when I came back, sure enough—he gave me a failing grade—because I'd missed some labs and classes."

Gmitter had plenty of credits to graduate from MCC at that point, but not enough credits for a degree in engineering. That prompted him to enroll in Utica Tech, where he redoubled his engineering efforts and earned his bachelor's degree in electrical engineering.

Becoming a test engineer at Harris

With his college and Navy experience behind him, Gmitter found himself employed as a TE 1 (for test engineer level 1) in product support at Harris, working with Falcon I systems. He was promoted to TE 2 level and became the lead engineer responsible for deployment of a test cell for the new Falcon II.

At that time, Harris had recently acquired a new building—the Carlson Road building—that would allow it to expand its manufacturing capacity to meet the growing demand for Falcon and other Harris products.

"We used to be a low-volume, niche, very customer-oriented division" known for quality and fast turnaround, Gmitter said. "But we started to produce in higher volumes, and as a test organization, we realized the deficiency of our standard platform, which was basically a one-at-a-time test system. We might be asked to test 10 products per day now on 10 test stations, but in six months, we might be asked to do 100 per day, requiring 100 test stations."

It became clear to engineering managers Ken Parfitt and Joseph Zingo that—to effectively use the manufacturing space the company had acquired—it would be necessary to develop a test strategy that would allow for faster and more flexible deployment of test stations. They promoted Gmitter to TE 3 and charged him with heading up the new-product-introduction (NPI) test group's efforts.

Gmitter and his team faced not only the challenge of expanding capacity. They also had to accommodate new modulation schemes and higher frequencies (up to 2 GHz on the forthcoming Falcon III vs. 512 MHz on the Falcon II multiband version). In addition, they had to find replacements for obsolete instruments and preserve 10 years worth of software-development effort, all while developing small-footprint test stations that wouldn't take up much production-floor space.

Essentially a player-manager in the process, Gmitter applied his knowledge of RF testing hardware and software architectures and leadership skills to build consensus among the NPI team and deliver upgraded


Your Search Is Over!

test stations, all within the tight timelines. He found no shortage of talent within the eight- to 10-member NPI test group. "We had a lot of type A personalities in one room who had a lot of great ideas. It could get tense and political," he said, with respect to whose idea would prevail. "When I came over, it was my job to oversee the overall direction, get these guys to come together, and be responsible for the final decisions."

Engineering manager Kenneth Parfitt recognized the need to revamp the Harris RF Communications test strategy to accommodate higher production volumes.

Developing a software strategy

The software strategy the team came together on is based on National Instruments' TestStand 3.1. "We had been using LabView for eight to 10 years and had looked at TestStand, but so far hadn't had a need for it. But after further review, we decided that, well, we could really start to take advantage of some of its key features, such as resource allocation, instrument locking, and parallel autoscheduling."

Choosing TestStand was only the beginning, however: "TestStand and LabView could do so many things that it was almost paralyzing." The challenge, Gmitter said, was basically "making a decision and putting a stake in the ground," defining what functions to implement immediately and what ones to save for later.

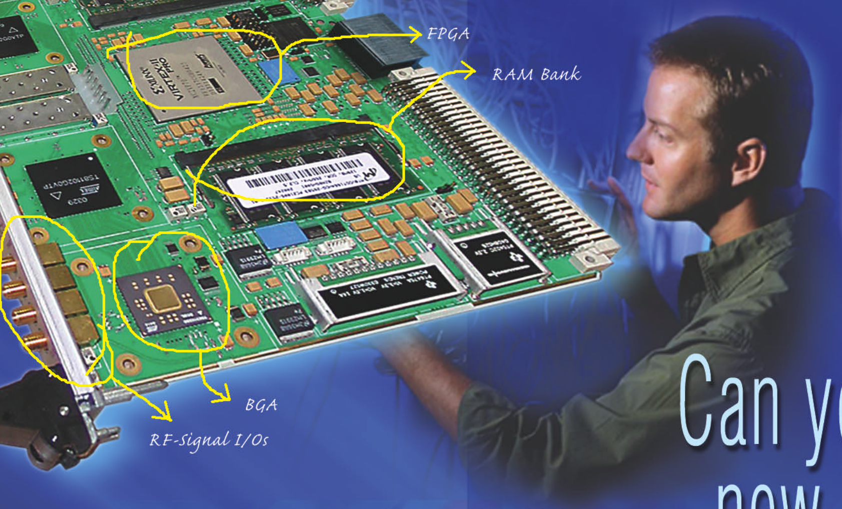
One goal of the team was to leverage its old software structure while eliminating some of the drawbacks. "For example, our instrument base structure had a handler and a driver; the top level was a handler, and every piece inside that handler had to be present on the hard drive and be executable, so it was really hard to get a station set up. You could be troubleshooting some digital I/O function that you would never use on the station, but if you didn't make it work, you couldn't use anything else. It was really difficult for someone to set up a station just to do a simple thing," he said.

Engineering manager Joseph Zingo charged Gmitter with the responsibility of guiding and focusing the talented engineers on the NPI test team.

FOREST MCMULLIN

"So, we decided we were going to change our driver-handler structure to a true object-oriented class-based structure." To that end, the team enlisted the help of an Endevo OOP wizard, which Gmitter described as a speedy class-based generation tool. The object-oriented programming approach enabled the team to detach functions from the lower-level software so they could execute only the functions they needed. "Everything didn't need to be present and executable, so if you had a simple function that you wanted to deploy in a half hour, you could do it pretty easily."

The team employed XML to describe test assets. "So that the test software knows what's connected to it, we implemented XML-based station-description documents. The station initialization software could read the XML files and say, 'OK, I know you have two PXI audio analyzers and a GPIB



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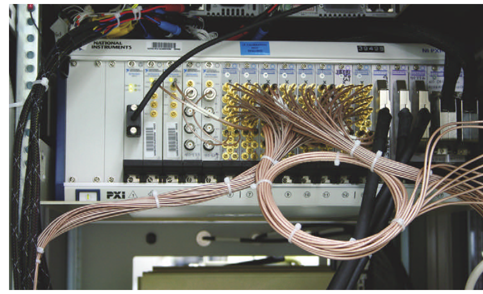
signal generator, and I know what the addresses are.' This allows our stations to be rapidly reconfigured or changed or edited in some way." To control source code during software editing, the team relies on Microsoft Visual SourceSafe.

PXI-based hardware

As for hardware, Gmitter's team focused on a PXI platform that allowed sufficient flexibility to accommodate legacy GPIB instruments as well as future USB and LXI instruments, should the need arise. A typical test station now might include NI PXI digitizers, Aeroflex PXI signal generators, Pickering PXI switches, Agilent GPIB signal analyzers, Anritsu GPIB RF power meters, Virginia Panel mass-interconnect hardware, and Cytec GPIB switching systems.

Commenting on PXI, Gmitter said, "I like what the PXI chassis does for us. It's overkill to begin with, but it always provides the ability for production to say, 'we were doing two a day but now we want to do 20 a day.' If you have a chassis there with spare slots and you designed your station such that it takes advantage of parallel processing, autoscheduling, and resource allocation, you can say, 'Station, I just plugged in two more audio analyzers,' or 'I put in two more signal generators. Please recognize them and make use of them.'"



PXI switch cards from Pickering Interfaces add flexibility to Harris test stations.

The trend for Gmitter's team is to adopt more PXI instruments as they become available—sometimes out of necessity. For example, he said, "Agilent discontinued its entire 89xx series of instruments. Fortunately, we found we could replace them with the NI PXI-5421 arbitrary waveform generator, PXI-4461 audio analyzer, and PXI-5660 modulation analyzer." Such substitutions aren't always ideal, he said, but satisfactory results can be had by making careful tradeoffs. For a spectrum analyzer, for example, such tradeoffs might involve resolution bandwidth, measurement speed, and dynamic range.

When asked if any one factor contributed most heavily to the project success, Gmitter said, "Teamwork. I just provided the direction and some of the technical expertise." As for winning the Test Engineer of the Year award, he said, "This is a credit not only to me but to all the engineers and managers at Harris that made the project possible. This was a tremendous team effort." T&MW

Test & MEASUREMENT WORLD

Signal Generation & Analysis for W-i-d-e-b-a-n-d Aerospace/Defense Systems

Choosing the right broadband measurement solution for your application

The ever evolving need for improved radar resolution, high data rate communications, and robust interference immune reception is the driving force behind the increase in wide bandwidth signals used in modern Electronic Warfare (EW), MILitary COMmunications (MILCOMS), ELectronic INTelligence (ELINT), and Direction Finding (DF) systems.

Finding instrumentation to test these ever evolving wideband aerospace/defense systems can be a challenge. Many of these advanced wideband systems are coherent multi-channel designs, employing phased array antennas that require multi-port test capability. Both wideband signal generation and analysis are needed, and with the current state-of-the-art, the wideband signal being generated or analyzed may be in a digital form rather than an analog form. As signal bandwidth exceeds 200 MHz, finding effective test equipment solutions for today's advanced RF system becomes increasingly difficult.

In this article, we look at some of the unique test instrumentation that is available to address the special needs of advanced aerospace/defense applications.

New Architectures to Meet the Challenge

Historically, these wideband test signal demands have required complex, custom-built test instrumentation.

Agilent now offers test equipment architectures with the features and interconnection ports needed to enable advanced wideband multi-port microwave signal generation and analysis.

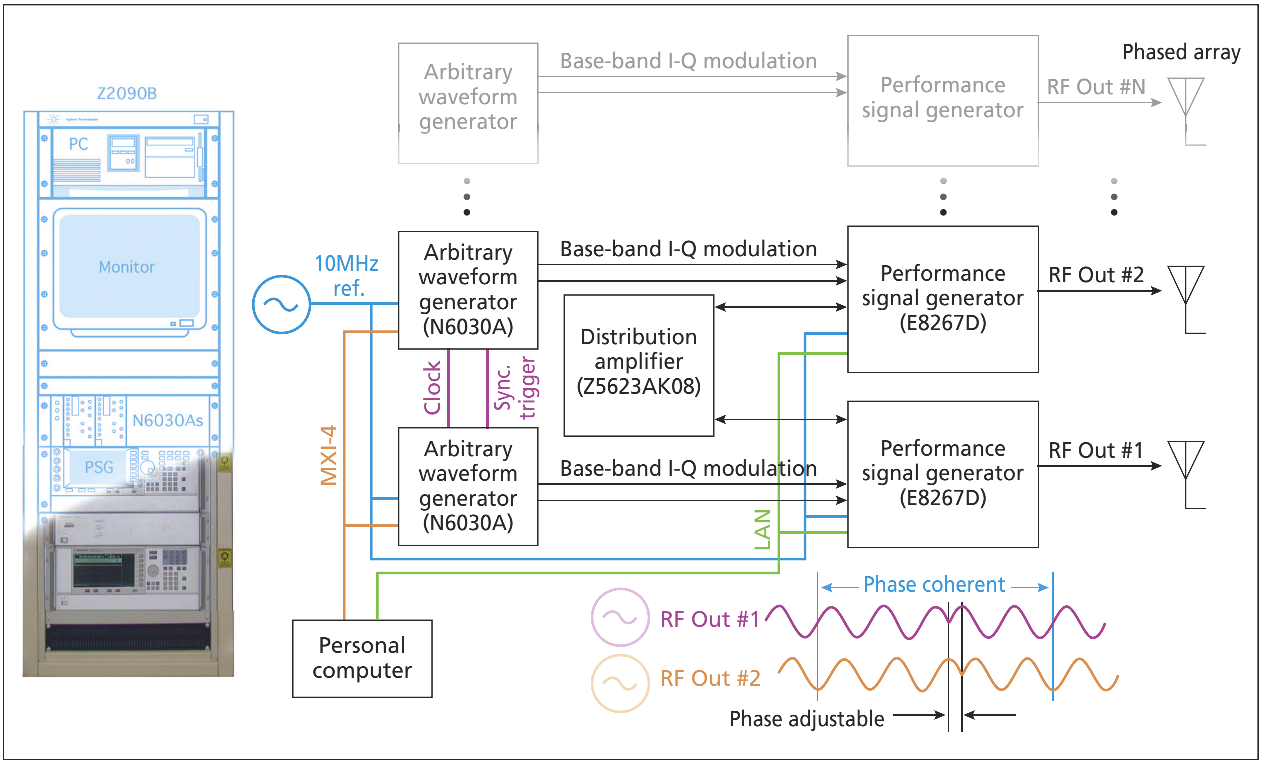


Figure 1: The Z2090B system can produce multiple modulated signal outputs that are phase coherent with precisely synchronized modulation patterns. This allows simulation of the spatial relationships of an arriving wave-front arriving at multiple antennas.

To illustrate, let's explore some of the specific test and analysis solutions beginning with signal generation.

Wideband Signal Source Solutions

Agilent's Z2090B wideband signal source solution utilizes the low phase noise E8267D Performance Signal Generator (PSG) and the high-resolution N6030A arbitrary waveform generator. The unique N6030A leads the industry with an amazing 15 bits of amplitude resolution at sample rates of 1.25 GS/s.

Working together, the 44 GHz PSG and high dynamic range N6030A arbitrary waveform generator deliver superb performance for a number of difficult wideband applications.

Phased Array & DF Testing

Agile phased array antennas dominate new designs, many of which operate over wide bandwidths. Testing the agile array's ability to track a target hundreds of miles away often requires a challenging test stimulus that is precisely phased across multiple channels to simulate an arriving wave-front.

Similarly, some intelligence receivers use multiple phase coherent receivers to determine the bearing angle to the signal emitter.

Testing these systems is difficult. Their wideband designs require precisely phased signal inputs at multiple input ports to simulate the spatial relationships of various emitters.

Field-testing multi-port electronic systems is often cost prohibitive as well, requiring expensive configurations of multiple airborne or surface assets spaced hundreds of miles apart.

Responding to this demand, the Agilent Z2090B system architecture is uniquely capable of addressing the challenges of Phased Arrays and DF equipment. Architectural interconnections have been provided to allow multiple PSGs to be modulated with multiple N6030A arbitrary waveform generators. The modulated outputs of the PSGs can then be connected to a phase coherent array. This arrangement can synthesize signal bandwidths up to 1 GHz from flexible digital files defined in Agilent's Signal Studio modulation synthesis tool.

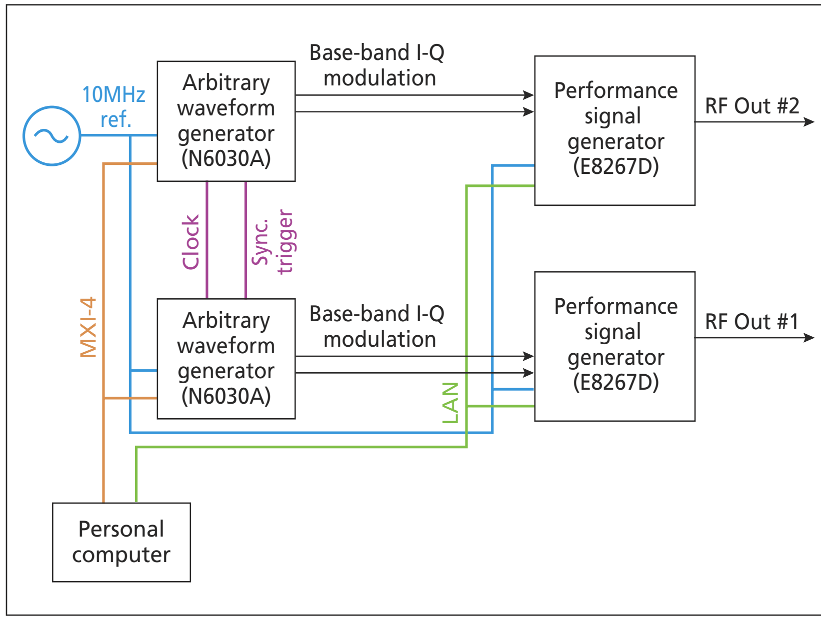


Figure 2: To generate entire spectral environments multiple N6030A arbitrary waveform generators can be up-converted to different frequency bands with the E8276D performance signal generators.

As signal bandwidth exceeds 200 MHz, finding effective test equipment solutions for today's advanced RF system becomes increasingly difficult.

The Agilent Z5623A distribution amplifier, along with a common 10 MHz reference locks the signal generators together to create a totally phase coherent set of signal outputs.

The system further enables full control over time, phase, amplitude and frequency. Synchronizing the arbitrary waveform generator clocks together, allows precise timing of modulated waveforms.

Phase offsets between multiple phase coherent signals from the 44 GHz E8267Ds are implemented using digitally synthesized modulation. This allows synthesis of complex signals arriving at antenna ports with the proper delays to simulate an arriving wave front.

Broadband EW Spectral Environments

Bandwidth requirements for military communications have also grown over the years as systems move from voice to bandwidth hungry high-resolution video.

Aerospace/defense systems typically function in complex RF spectral environments, with jammers and interferers that utilize many octaves of bandwidth. Compounding the growth in data rate, many communications systems have gone to spread spectrum signals that frequency hop over huge bandwidths to reduce the probability of intercept and improve performance in messy signal environments.

Generating gigahertz of spectral environment to test the robustness of these data links can require extreme bandwidth capability.

When confronted with the need to generate such a test environment, multiple PSGs modulated with N6030A arbitrary waveform generators can be offset in frequency to provide continuous signal bandwidths greater than the 1 GHz available with a single PSG and N6030A system.

For example, five PSGs and N6030As can generate up to 5 GHz of spectrum to test a broad range of spectral situations.

Furthermore, the N6030A's superior sequencing ability allows it to create complex signals using sequencing of short repetitive signal snippets without massive amounts of signal memory. This important feature enables long or continuous play of wide bandwidth spectral environments, without Tera bytes of high-speed waveform storage memory.

In addition, the N6030A incorporates a built-in Direct Digital Synthesis (DDS) feature that expands simulation capabilities without using additional memory.

The Z2090B can also be configured to playback wideband signal recordings taken from the field. MILCOM engineers can employ the Z2090B to analyze system responses to multi-path, interference and more, using either recorded or synthesized signals.

Advanced tools, like Signal Studio or third party software solutions, can quickly and easily generate complex multi-carrier spectral environments that include moving emitters with changing Doppler shifts.

The Agilent Z2090B series signal simulation systems offer the flexibility and performance for addressing challenging wideband signal stimulus requirements.

Broadband Signal Analysis Options

Many of the same challenges that exist for creating test signals exist for analyzing broadband modulated signals: bandwidth, multi-port capability, coherency and the like, all present measurement challenges.

For this reason, Agilent offers a variety of signal analysis options for broadband system analysis and test.

Coherent Receiver Array Measurements

Whether comparing the phase of arrival of two complex modulations to resolve a bearing angle or characterizing the spectral shape of an Ultra Wide Band (UWB) signal, the Infiniium Oscilloscope offers a tremendous variety of wideband measurements.

Agilent's Infiniium 80000B series oscilloscopes sample at rates up to 40 GS/s, providing analysis bandwidths up to 13 GHz wide. Furthermore, the 80000B has the industry's lowest noise floor, best phase noise performance and the flattest frequency response.

These superior performance traits allow the multi-channel Infiniium oscilloscope to capture ultra narrow time domain events and conduct RF modulation analysis.

The 'VSA 80000A Ultra Wideband Signal Analyzer,' bundles the Infiniium 80000A oscilloscope with the 89600A Vector Signal Analyzer (VSA) software. This powerful combination expands the Infiniium's measurement capability far beyond traditional time domain measurements. The VSA software enables frequency domain spectral measurements as well as in depth modulation measurements.

In addition to performing these measurements on signals with many gigahertz of bandwidth, the multiple input ports of the high-speed oscilloscope allow simultaneous two-channel analysis.

Even cross channel signal correlations and phase measurements can be made. These unique capabilities are ideal for comparing the phase differences between two different wideband receiver channels.

The VSA 80000A's unique wideband two-port measurement capability makes it an effective measurement solution for advanced wideband multi-channel systems.

Field-testing multi-port electronic systems is often cost prohibitive as well, requiring expensive configurations of multiple airborne or surface assets spaced hundreds of miles apart.

Software Defined Radios

When considering broadband signal measurement capability, logic analyzers may not immediately come to mind; however, with the ubiquitous trend to implement greater portions of complex systems in software defined hardware with ultra fast FPGA digital processing, increasingly the wideband signal is digital rather than analog.

The Agilent analysis product line is unique in that the 89600A VSA software is available on a variety of hardware platforms. Spectrum analyzers, oscilloscopes and logic analyzers can all host this powerful analysis tool.

The Agilent 16800 series logic analyzers, for example, support measurement of wideband modulations in digital formats with the 89600A VSA software.

Not only do these high speed wide bandwidth logic analyzers provide a means to measure digital signal modulation performance while still in a binary bus format, but the 89600A software interface is identical to that used on Infiniium oscilloscopes and traditional vector signal analyzer instruments.

The 89600A analysis software can then be applied to vastly different signal formats. Logic analyzers can perform modulation analysis on digital I–Q busses. Even bus signals deep inside Field Program-

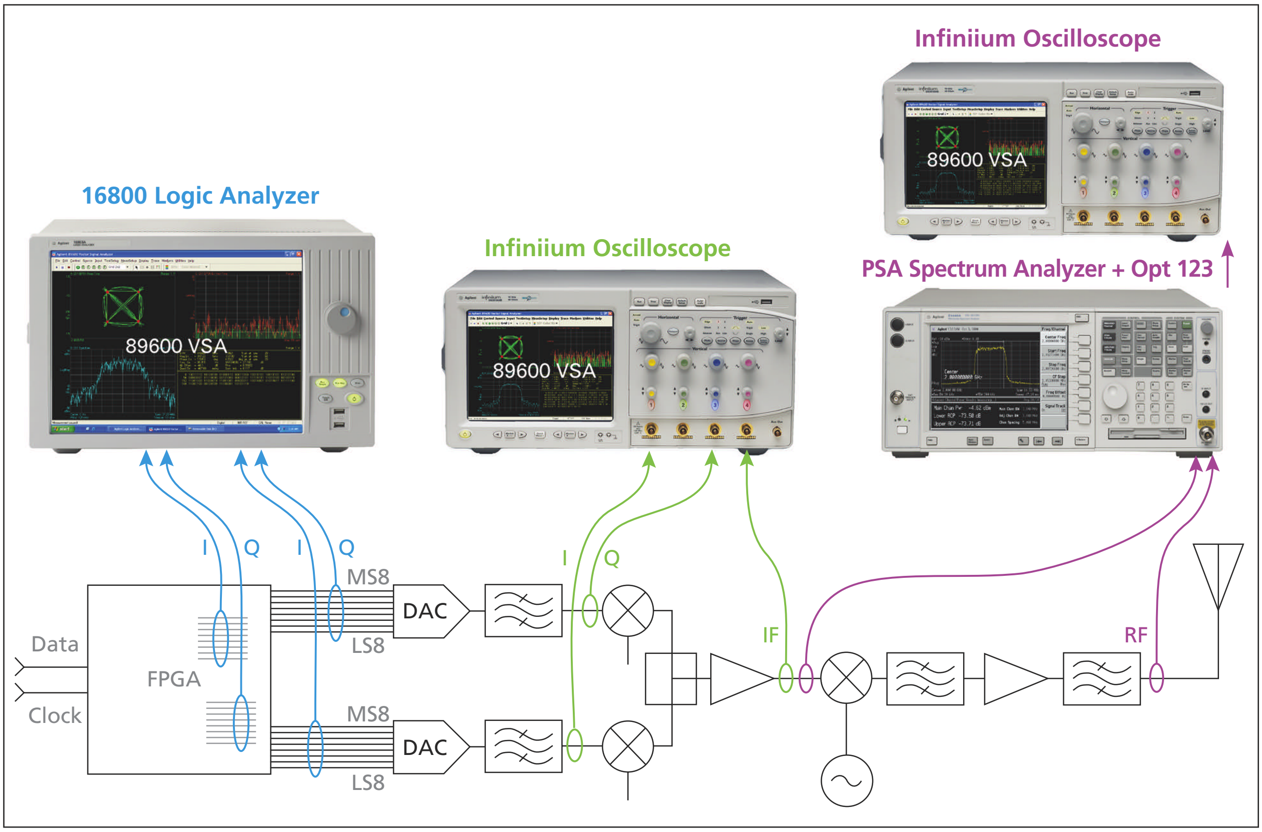


Figure 3: Agilent offers a unique set of wide bandwidth analysis tools that all use the powerful 89600A vector signal analyzer software. High-speed logic analyzers, broadband oscilloscopes and high performance spectrum analyzers allow consistent detailed modulation analysis, no matter what signal format is used.

mable Gate Arrays (FPGA) can be probed with Agilent's FPGA dynamic probing.

The view scope function coordinates precision timing of the logic analyzer and oscilloscope signals on a single screen, to reveal the exact digital bus state of signal errors found with the 89600A VSA software.

The MXA or E4440 PSA series of Performance Spectrum Analyzers (PSA) also support the same 89600A software, allowing uniform analysis of all types of signal formats at vastly different frequencies and with vastly different signal formats. Now, one consistent set of analysis software can compare modulated signals across digital and analog format transitions.

For wideband analysis the PSA spectrum analyzer with option 123 can function as a broadband downconverter whose IF output can be digitized using the Infiniium oscilloscope to achieve measurement bandwidths up to 230 MHz throughout the PSA's frequency range of 3 Hz to 50 GHz. Other external down-converters can be used for wider bandwidths.

This combination coupled with the 89600A VSA software provides a powerful measurement tool for broadband MILCOM signals as well as characterization of radar pulses containing complex intra-pulse modulation.

Outlook

Agilent offers the wideband measurement solutions needed to extend performance far beyond typical test instruments.

Whether the requirements are for radar, EW, ELINT, phased arrays, or just terrestrial Ultra Wide Band (UWB) communications, the Z2090B provides a test stimulus platform for wideband success.

The advanced measurement capabilities of Agilent's 89601 VSA software and a variety of hardware front ends ranging from the E4440 PSA, Infiniium oscilloscopes to the 16800 series logic analyzers, can tackle tough wideband, coherent multi-port analysis problems.

Agilent would like to help. Supported by factory experts, the Agilent field representative is trained to assist you in selecting the right broadband stimulus and analysis test solutions for demanding aerospace and defense applications. ■

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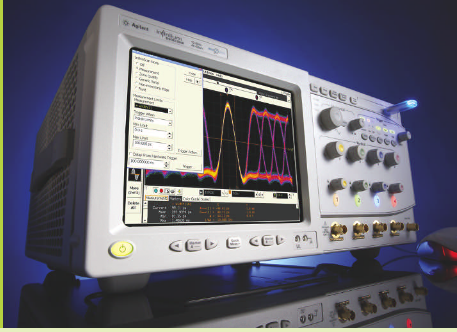

Test & Measurement World's readers have selected the Agilent 80000B oscilloscope as the Test Product of the Year. Courtesy of Agilent Technologies.

High-bandwidth scope TAKES THE PRIZE

MARTIN ROWE, SENIOR TECHNICAL EDITOR

Covering from what is now midrange to almost the top end for bandwidth, the Agilent Technologies 80000B series of real-time oscilloscopes has been selected as the 2007 Test Product of the Year by a vote of *Test & Measurement World*'s readers (www.tmworld.com/awards). The 80000B series instruments are unique in that they let you buy just enough bandwidth for your current application and then let you upgrade through software code when the need to test faster signals arises.

Eight models cover the range of 2 GHz to 13 GHz. Why so many options? "Capital budgets are tight these days," said product manager Lon Hintze. "It takes almost an act of Congress to get approval for new test equipment. So, we wanted to give engineers the option of buying just enough scope for today's jobs without forcing them to buy a new scope next year."

The different bandwidth models are aimed primarily at different serial buses. For example, the 2-GHz model is used for FPGA development where data rates run from 500 Mbps to 1 Gbps. The 4-GHz model works for 1.25-Gbps signals. At the top end, the 12-GHz model finds use in PCI Express 2 (5 Gbps) and the 13-GHz model is used for SATA 3 (6 Gbps).

Engineers at Agilent's Colorado Springs facility designed the 80000B oscilloscope line. Courtesy of Agilent Technologies.

Beyond analyzing serial buses, engineers also use the 80000B scopes for aerospace, defense, and RF applications. The scopes are fast enough to directly digitize an RF carrier—no down-converter required. They can also measure laser pulses, neutrino emissions, and electrostatic discharge and electromagnetic interference.

Engineers have already taken advantage of the 80000B bandwidth upgrade since it was introduced in February 2006. "The first came about six months after introduction," said Hintze.

Of course, the wider a scope's bandwidth, the wider a range of noise it can capture. "If you 2X bandwidth, you 2X noise," said Agilent R&D project manager Mike Karin. "We needed a new approach to reduce noise." That approach resulted in an RF package that has built-in Faraday shields around the scope's sensitive analog pre-amp and trigger circuits. Agilent engineers created "RFI chambers" to suppress external noise. A new SiGe buffer amplifier, developed for the 12-GHz and 13-GHz models, also lowers noise over those used in previous scopes.

When developing the 80000B, the design team, based in Colorado Springs, CO, leveraged knowledge from other parts of the company. The 20-Gsample/s analog-to-digital converters (ADCs) were developed at Agilent Labs, in Santa Clara, CA. The RF package design came from the company's Microwave Technology Center in Santa Rosa, CA. This package consists of two printed-circuit boards (PCBs) with solder "walls" in between. The Faraday cages are formed when these two boards are soldered together. The package mounts to the main PCB using a surface-mount technology process.

The Agilent engineers in Colorado Springs also developed a new probe tip topology that raised the bandwidth of the probe tips to 13 GHz, and they designed a new SiGe probe amplifier for the 13-GHz probes. In addition, they developed and built the thick-film substrate used to hold the probe's amplifier close to the measurement point.

What has drawn engineers to the 80000B line? Hintze points to three factors: signal integrity, because of the scope's low noise floor; probing, because of the digital signal processing (DSP) compensation that results in flat frequency response; and a wide variety of application packages including 12 compliance packages for serial buses and jitter analysis. T&MW

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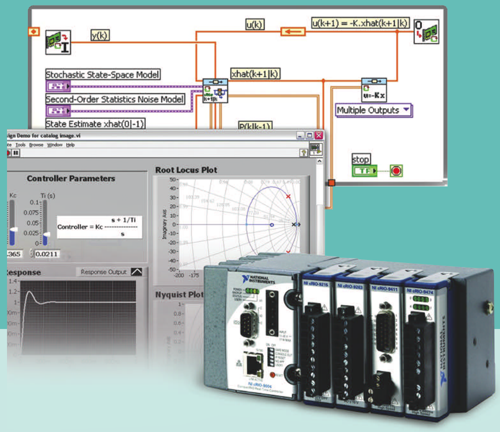


The 20th anniversary edition of LabView, introduced in 2006, offers extensive features and works with many hardware platforms, yet it maintains the intuitive, easy-to-use data-flow graphical environment of LabView 1. Courtesy of National Instruments.

Graphical programming for test and measurement

RICK NELSON, CHIEF EDITOR

In 1986, graphical programming burst upon the test-and-measurement scene with the introduction of National Instruments' LabView. Created by NI co-founder Jeff Kodosky (who now serves as NI business and technology fellow), LabView helps engineers and scientists in diverse industries quickly produce the code necessary to run a wide range of applications.

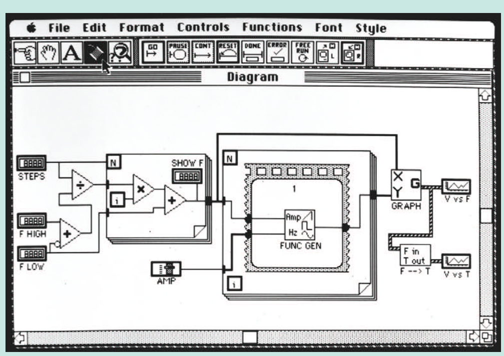
In the 20 years since its debut, the LabView graphical programming platform has revolutionized the development of scalable test, measurement, and control applications. In recognition of LabView's longevity, ease of use, market penetration, and ever-increasing sophistication, *Test & Measurement World*'s editors have chosen to honor it with the 2007 Test of Time award, which recognizes a product that continues to provide state-of-the-art performance for at least five years after its introduction.

Offering an intuitive graphical development similar to flowcharting, LabView challenged traditional text-based approaches to programming, enabling programmers to "wire" together virtual instruments on their computers just as they would wire actual instruments in the lab. The original LabView version ran on Macintosh computers, and the August 2006 introduction of the latest, 20th anniversary version—Labview 8.20—was accompanied by a LabView 1 demonstration on a dusted-off '80s-era Mac.

Since the 1986 debut, LabView has been ported to Sun and Windows platforms (those versions appeared in 1992), and you can find versions that work with personal digital assistants, field-programmable gate arrays, and embedded digital signal processors. And LabView is not all work and no play—National Instruments worked with Lego to develop the LabView-programmable Lego Mindstorms NXT robots.

Commenting on the Test of Time award, Dr. James Truchard, National Instruments' president, CEO, and co-founder, said, "Just over 20 years ago, we set out on a quest to do for test and measurement what the spreadsheet had done for financial analysis. The result was LabView—a graphical programming environment that has stood the test of time for test-and-measurement applications and gone on to become a graphical system design tool for designing and prototyping complex systems for deployment in industrial applications."

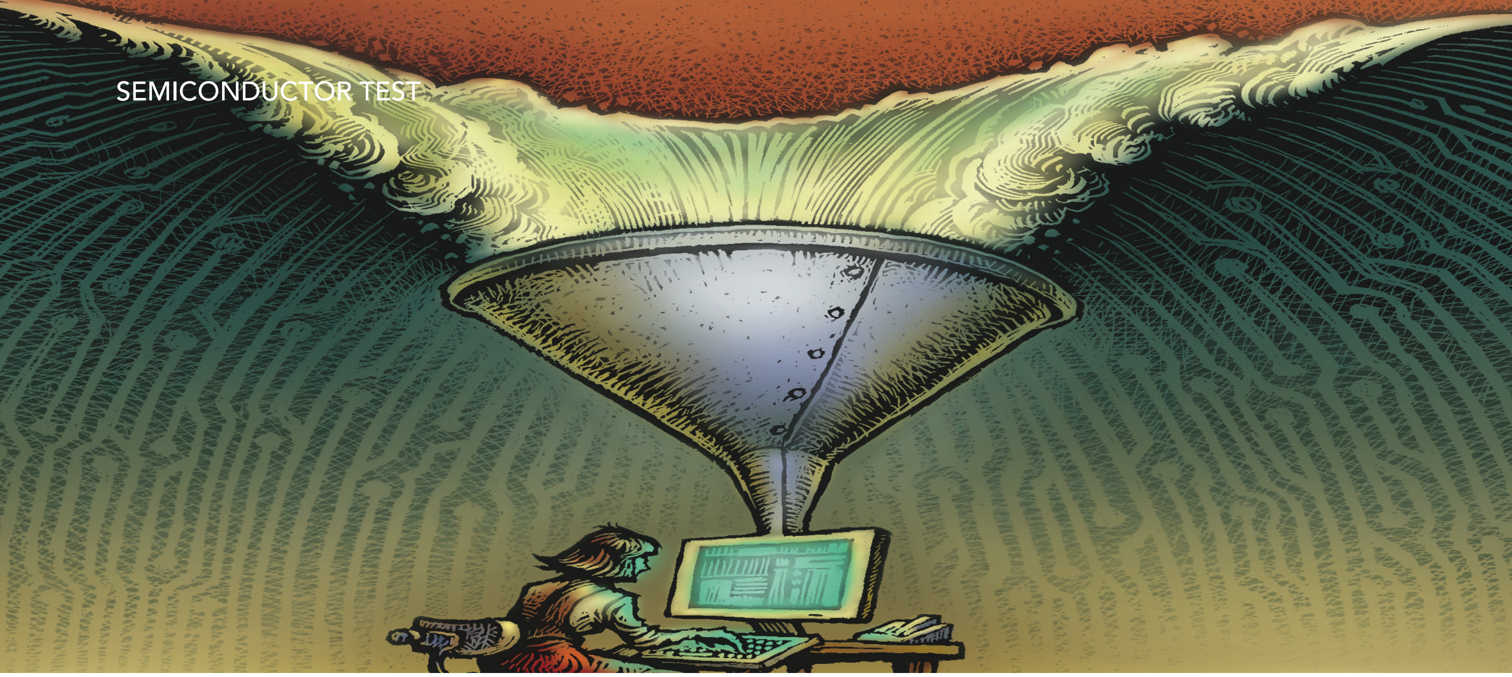
During the introduction of the 20th anniversary edition, which occurred during NIWeek 2006 in Austin, Dr. Truchard explained his vision for LabView 8.20: It combines text-based math, supports various models of computation, and makes it easy to build embedded applications, all in the support of a three-pronged attack addressing design, prototyping, and deployment. LabView 8.20's capabilities are based on the underlying hardware capabilities, he said, adding, "New high-bandwidth buses, such as PCI Express, are giving virtual instrumentation and desktop computers the power to process enormous amounts of complex IF and RF data in communications applications. With LabView 8.20, engineers can intuitively develop design models and measurement applications through a graphical-programming notation that naturally represents the data flow of communications systems."



LabView 1 brought graphical data-flow programming for test-and-measurement applications to the Macintosh computer in 1986. Courtesy of National Instruments.

LabView 8.20 includes an object-oriented programming environment, a DLL import wizard, an FPGA wizard, a Web services wizard, a LabView instrument-driver export wizard, and a math-script capability that allows existing scripts to be easily used within LabView programs. In addition, a new modulation toolkit provides a software-defined approach to communications system design and test.

As for future versions, Truchard said that programming languages typically have life spans of about 50 years, so LabView users can expect to see another 30 years of innovation. T&MW



OPTIMIZING COMPRESSION

IMPLEMENTING SCAN COMPRESSION ON-CHIP PROVIDES SIGNIFICANT TEST COST SAVINGS, BUT HOW MUCH COMPRESSION IS ENOUGH?

CHRIS ALLSUP,
SYNOPSYS

In the 1990s, Carnegie Mellon researchers created a comprehensive scan-test cost model that demonstrated how design for test (DFT) contributes to profitability (Ref. 1). With scan compression in wide use, it is time for a new economic model, consistent with the earlier framework but focused on scan compression, not just scan. To that end, I have developed an economic theory (Ref. 2) that unifies test data reduction and time reduction concepts and considers the impact of test pattern inflation.

I have written in these pages previously (Ref. 3) on test application time reduction (TATR), which along with test data volume reduction (TDVR) has diminishing returns as compression increases (Ref. 4). TATR is an asymptotic function. For a scan-compression factor of x (assuming the scan chains are well balanced with no pattern-inflation issues), TATR can be expressed as:

$$\text{TATR} = 100\% \bullet (1 - 1/x)$$

Therefore, at 50X compression, you can expect at most a 98% test time reduction: 100% • (1 – 1/50) = 98%. And at 100X compression, you can expect at most a 99% test time reduction: 100% • (1 – 1/100) = 99%.

An optimal compression level, λ, minimizes the total costs of test and, consequently, maximizes profits. Above this optimal compression level, the total costs of test gradually increase again. In **Figure 1**, the x-axis represents the ratio

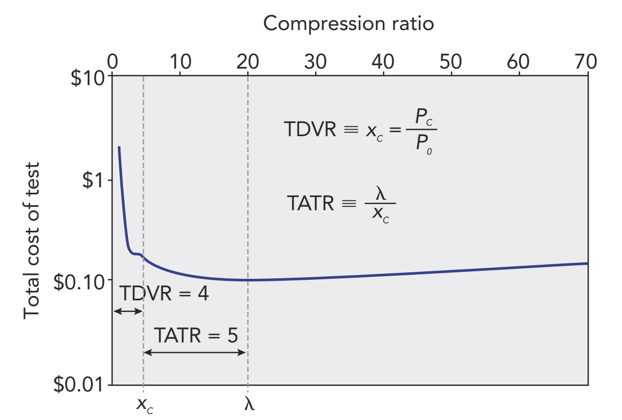
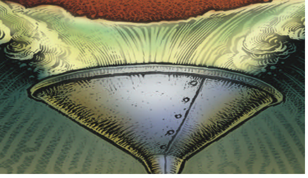


FIGURE 1. An optimal compression level, λ, minimizes test cost. x_c is the compression level needed to fit a complete scan ATPG pattern set, P_c, into the fixed amount of tester memory. TATR denotes the economic benefits of increasing compression up to λ.



of the number of internal scan chains to the number of external scan chains.

In this article, I address the cost impact, in terms of dollars per good die, on digital-scan tests that employ automatic test pattern generation (ATPG), with respect to the following major cost components of test:

- **Cost of field escapes** (C_{ESC}) is the cost of defective ICs that are incorrectly identified as good parts, so they "escape" to the field. (You can also consider the cost of escapes going from, say, wafer probe to system-level test). If your pattern set doesn't fit within tester memory, you can use compression to significantly reduce this cost.
- **Test execution cost** (C_{EXEC}) is the cost directly related to the test cycle count and the tester time spent running ATPG patterns. Compression can decrease this cost, although not always.
- **Silicon area overhead cost** ($C_{SILICON}$) consists of the cost of the scan-compression circuits and interconnects in your design. This cost is proportional to the amount of compression in a design.

In addition, there are two costs that are less affected by compression:

- **Cost of test preparation** (C_{PREP}) is the engineering, compute-resource, and tool costs related to preparing ATPG test patterns. Establishing a meaningful relationship between the scan-compression level and C_{PREP} is difficult. For automated scan compression, there is not a large impact on C_{PREP} in going from, say, 10X compression to 50X compression.
- **Cost to diagnose failed parts** (C_{DIAG}) can be significant, especially for highly compressed designs that you debug manually. But as with C_{PREP}, C_{DIAG} is difficult to quantify in terms of compression level. Because automated tools are getting better at diagnosing compressed designs, this cost is relatively insensitive to compression level.

Consequently, the only reason to implement scan compression is to reduce C_{ESC} and C_{EXEC}, but you must keep in mind that any increase in compression also increases the expense of $C_{SILICON}$.

TDVR and TATR revisited

TDVR can *only* reduce the cost of escapes, and TATR can *only* reduce test execution cost. To understand why, consider a complete high-fault-coverage ATPG pattern set. Call the number of patterns P_C, in which "C" denotes "complete." Also assume that you can't fit the entire pattern set into the tester memory, *M*, allocated for ATPG stimulus and response patterns, so you must use compression.

To load a subset of these patterns into tester memory, you need to compress by exactly the amount of test data volume corresponding to the pattern level, *P*, divided by *M*. This is just the ratio of *P* to P_0, the number of patterns you can load into memory without compression:

$$x = \frac{P}{P_0}, \qquad P_0 = \frac{M}{3F} \qquad (1)$$

where *F* is the number of scan flops in the design. The coefficient 3 represents one scan stimulus bit, one response bit, and one mask or measure bit to determine if the response bit should be compared or not. For each unit increase in compression, you can load P_0 additional patterns from the complete set into memory.

Somewhere between "no compression" and a high level of compression lies x_C, which represents the level needed to fit the complete scan ATPG pattern set, P_C, into the fixed amount of tester memory. The "TDVR phase" is defined as the range of compression that extends up to this compression level, $x_C = P_C/P_0$. Increasing compression above this level has no economic benefit in terms of reducing the cost of escapes, because there are no additional patterns being loaded to improve quality.

Above x_C, however, you do have potential cost savings from TATR, because the scan-chain lengths continue to decrease with higher compression. You can define compression higher than x_C as the "TATR phase."

In this phase, you can continue increasing compression up to λ, above which the area overhead cost of compression exceeds the benefit of decreasing test application time. The maximum TATR that is economically viable is the ratio of λ to x_C.

(continued)

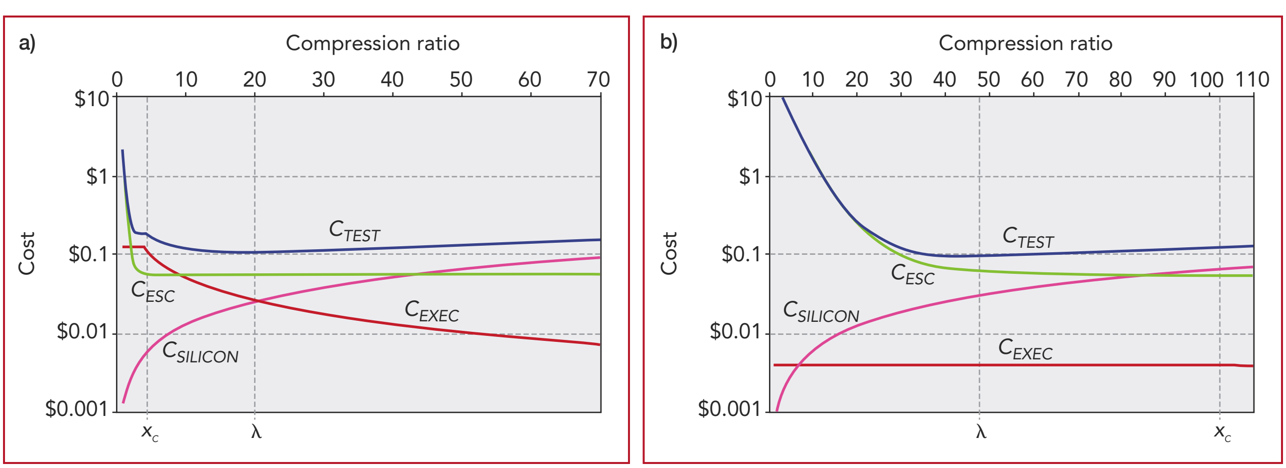


FIGURE 2. a) If λ is greater than x_C, then you know there are cost savings to be gained by increasing compression to reduce tester time. b) Alternatively, if you find that λ is less than x_C, you know that the most cost-effective compression strategy is to simply truncate the patterns.

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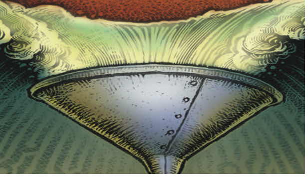

In Figure 1, the TDVR phase extends to 4X compression. The TATR phase starts at 4X, and the maximum cost-effective TATR is at 20X, but this doesn't imply a 20X, or even a 16X, test time reduction. Instead, you get 5X, or an 80%, reduction in test time, which works out to be exactly the ratio of the test cycle count at 20X and at 4X compression. The graph indicates that compression decreases the total costs of test by about 95%, with all but 4% of this reduction occurring in the TDVR phase.

To understand the disparity in cost reduction between TDVR and TATR, I'll now examine the impact that compression has on the three component costs of test that are highly sensitive to compression level.

Impact of compression on cost of escapes

The following exponential approximates the convergence of fault coverage vs. pattern count using an ATPG tool, especially in the high-coverage region:

$$f(P) = f_C(1 - e^{-\eta P}),$$
$$\eta = -\frac{\ln(\Delta)}{P_C} \qquad (2)$$

where f_C represents the maximum measured fault coverage of the complete pattern set, P_C, and Δ is the difference between f_C and the maximum predicted fault coverage. The smaller Δ is, the larger the exponential constant, and the faster the convergence.

Recall that compression in the TDVR phase is just the ratio of the pattern count, P, to the number of patterns you can load into tester memory without compression, P_0. Therefore, if you substitute xP_0 for P in the exponential formula, you can describe the fault coverage as a function of compression, and the exponential constant is simply scaled by P_0.

Once you have fault coverage as a function of compression, you can describe the escape rate using the Williams and Brown formula (Ref. 5) that expresses escape rate as a function of fault coverage and yield. The cost of escapes, at the least, will be the cost to manufacture and test these escapes.

Keep in mind, however, that the cost of escapes can actually be higher. The Carnegie Mellon cost model uses a parameter α_{ESC} to account for this escape-multiplier effect at any given stage of the test process. The higher the multiplier, the greater the cost of escapes across all compression levels.

As you increase compression, the cost of escapes drops off logarithmically as the additional patterns loaded into tester memory detect more faults, until all the patterns are loaded at x_C. Above x_C, the TDVR phase ends, and there is no further decrease in the cost of escapes; the curve is flat, as illustrated in **Figure 2a**.

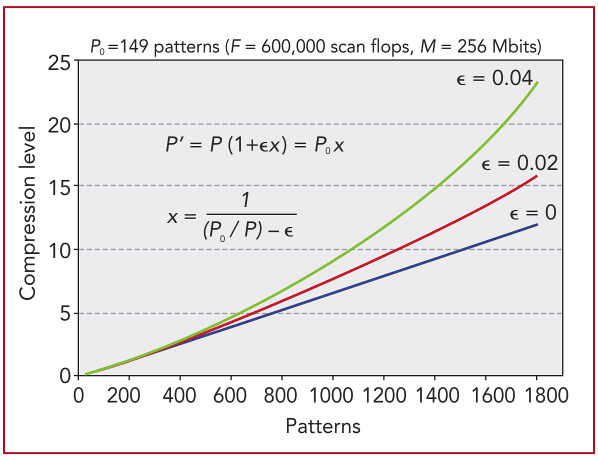

FIGURE 3. For any pattern level, the compression level increases relative to the baseline condition without pattern inflation.

Impact of compression on cost of test execution

Test execution time is constant during the TDVR phase, because every unit increase in compression adds another P_0 number of patterns that must be tested, which exactly offsets any potential test time reduction. This test time is approximately T_0, the time it takes to execute all P_0 patterns on the tester without compression:

$$T_0 \cong \frac{P_0 F}{C f_{TEST}} \qquad (3)$$

where C is the number of scan I/O channels (or external scan chains) and f_{TEST} is the tester scan-shift frequency. Above x_C, tester time declines by a factor of x_C/x, as shown in Figure 2a.

Impact of compression on the silicon area overhead cost

Independent of the compression phase, the silicon area cost will continue to increase as you increase the number of scan chains for compression. A simple linear formula that represents the circuit die size as a function of compression (Ref. 3) can model this increase. You can measure the slope, γ, of this area increase empirically or use a ratio-of-gates approach, given by:

$$\gamma = \frac{gC}{G_0} \qquad (4)$$

where g is the number of compression-circuit gates added per scan chain, G_0 is the total number of gates in the design without compression, and C is again the number of scan I/O channels.

It's useful to introduce a second-order area-scaling factor, ζ, to model a nonlinear area increase that can occur with higher compression. Even if the added gates per scan chain remains constant, wire-routing congestion at higher scan levels could increase the silicon area more than the linear formula predicts.

Note that higher values of γ and ζ tend to work against compression, lowering λ. The silicon cost is displayed in Figure 2a. As you approach 100X compression, the cost increases by about two orders of magnitude, as expected.

Finding the optimal compression level

You can apply this methodology and these equations to find the optimal compression level. Start by running ATPG to measure the fault coverage as a function of pattern count. Next, derive the exponential constant, η, to curve-fit $f(P)$ in equation 2 to your data using appropriate values of Δ. Finally, calculate the optimal compression level, λ, that minimizes the total cost:

$$C_{TEST} = C_{ESC} + C_{EXEC} + C_{SILICON}$$

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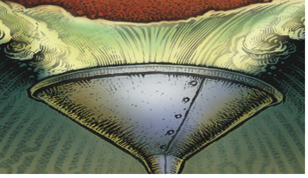

implementing the most cost-effective compression strategy. If you calculate λ and it is identical to x_C, then you compress all the ATPG patterns knowing you have minimized the costs of test.

If you estimate that λ is greater than x_C, then you know there are cost savings to be gained by *increasing compression to reduce tester time*. Use the following equation to calculate λ exactly (**Table 1** defines the parameters):

$$\lambda = \sqrt{\frac{R_{ACT}T_0\alpha_0}{C_S A_0 \gamma(2 - Y_0)}\left(\frac{P_C}{P_0}\right)},\ \lambda > x_C \quad (5)$$

Say you need to apply a certain level of compression $x_C = 4$ to fit the complete pattern set into tester memory and your calculated value of λ is 20, greater than x_C. You'll want to increase compression to $x_C = 20$ to take full advantage of more cost savings from test time reduction. λ occurs where the cost derivatives for the silicon area overhead and the test execution time are equal. Note that the fault coverage and the escape multiplier don't even factor in, because the cost of escapes is flat during the TATR phase and has no impact on λ when it is greater than x_C.

Alternatively, if you estimate that λ is less than x_C, you can calculate it as follows:

$$\lambda = -\frac{1}{\eta P_0}\ln\left(\frac{-\gamma(2 - Y_0)}{\alpha_{esc}\ln(Y_0)\eta P_0}\right),\ \lambda \leqslant x_C \quad (6)$$

In this case, you *truncate the pattern set*. In this situation (**Figure 2b**), all patterns, P_C, can be loaded into tester memory by compressing to 103X. But compressing more than λ = 47 just increases costs, so there is no economic benefit gained by compressing any higher.

λ occurs where the cost derivatives for silicon area overhead and escapes are equal. Although the cost of escapes is sensitive to the maximum fault coverage, f_C, the cost derivative always occurs in the high-coverage region and is therefore insensitive to f_C as long as fault coverage is high. In this case, λ is nearly independent of f_C.

Pattern inflation

So far, I have ignored the phenomenon of pattern inflation caused by compression. But you really can't disregard it, because the higher the compression level, the more patterns that ATPG produces. Although linearity of pattern inflation is not a strict requirement for this economic model, in-house experiments on many designs have revealed that pattern inflation behaves linearly across a wide range of compression levels. You can describe the effects of pattern inflation using a parameter, ϵ, that represents the fractional increase in pattern count per unit increase in compression.

First, examine the effect pattern inflation has on TDVR. Remember that in the TDVR phase, the compression level is just the ratio of the number of patterns, P, that fit in memory at this level to the number of patterns, P_0, that fit in memory without compression. It follows that for any pattern level, the compression level increases relative to the baseline condition without pattern inflation in the manner displayed in **Figure 3**. Essentially, more compression is needed to load the same amount of patterns into tester memory than before.

This implies that x_C also increases with pattern inflation. For a design with λ in the TATR phase, sufficiently high ϵ can increase x_C above the predicted value of λ in equation 5. The result is that test time reduction is no longer cost effective, and you will find it more beneficial to compress to the level x_C or less. To determine how much to compress, solve the following formula for x:

$$\frac{x}{1 + \epsilon x} + \frac{2\ln(1 + \epsilon x)}{\eta P_0} = \lambda_{\epsilon=0} \quad (7)$$

where the right-hand side represents equation 6, the formula for $\lambda \leqslant x_C$ that assumes zero pattern inflation. The magnitude of λ in the TDVR phase will be higher when you account for pattern inflation than that predicted by equation 6. Note that it's easy to solve equation 7 by obtaining the intersection of the curves corresponding to each term.

Now, examine the effect pattern inflation has on TATR. Pattern inflation increases the TDVR phase. The effect of an increase in x_C, however, is completely offset by a corresponding decrease in the rate (per unit increase in compression) of test time reduction due to the pattern-inflation term, $1 + \epsilon x$. Therefore, while pattern inflation increases the execution cost, there is no net change in the magnitude of λ.

(continued)

Table 1. Parameters affecting optimal compression level

Compression	x_C	$\lambda < x_C$	$\lambda > x_C$
Process		Y_0	Y_0
Design	F	F, A_0	F, A_0
DFT	P_C, ϵ	P_C, ϵ, γ, ζ, η, f_C	P_C, γ, ζ, C
Tester	M	M	f_{TEST}
Const infrastructure		α_{ESC}	C_S, R_{ACT}
Strategy		Truncate patterns	Reduce test time

(Parameters in red have a positive correlation; those in blue have a negative correlation.)

Parameter definitions

α_{ESC}	Escape-rate multiplier
γ	Scan compression area-scaling factor
ϵ	Pattern inflation factor for compression
ζ	Second-order area scaling coefficient
η	Exponential constant affecting fault-coverage convergence
A_0	Die area without compression
C	Number of external scan chains or scan I/O pairs
C_S	Silicon-area cost multiplier
F	Number of scan flip flops
f_C	Fault coverage of complete pattern set
f_{TEST}	Tester scan-clock frequency
M	Memory allocated for stimulus/response patterns
P_C	Scan ATPG pattern count before inflation
R_{ACT}	Cost of active tester
Y_0	Manufacturing yield

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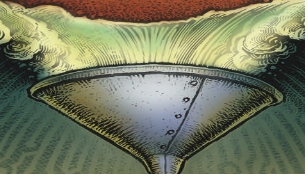

You can thus use simple criteria to decide if you even need to account for pattern inflation to determine the optimal level of compression. If λ is much larger than x_C with no pattern inflation, then there is a strong likelihood that it will still be larger than x_C even after pattern inflation is factored in. Equivalently,

$$\text{If } \frac{\lambda}{P_C/P_0} >> 1 \text{ then } \lambda \text{ is independent of } \epsilon \quad (8)$$

If this condition is true, you need not measure ϵ. If the condition is false, then you need to extract the value of ϵ to find λ using equation 7. To do this, run ATPG on your design with several different compression levels. **Figure 4** plots pattern count vs. compression for an industrial design implemented at five different compression levels, where each point corresponds to the same fault-coverage level.

Once you calculate the least-squares curve fit, ϵ is the ratio of the line's slope to its y-intercept. Subsequently, use the y-intercept in the formulas instead of P_C.

In summary, most savings from compression arise from either TDVR or TATR. If you must compress your patterns to load them into memory, then TDVR will be the dominant factor contributing to savings and you can use even more compression to derive incremental savings from test time reduction. Conversely, if most of your patterns fit into memory without compression, then TATR savings can be significant, especially if you have few scan I/O channels.

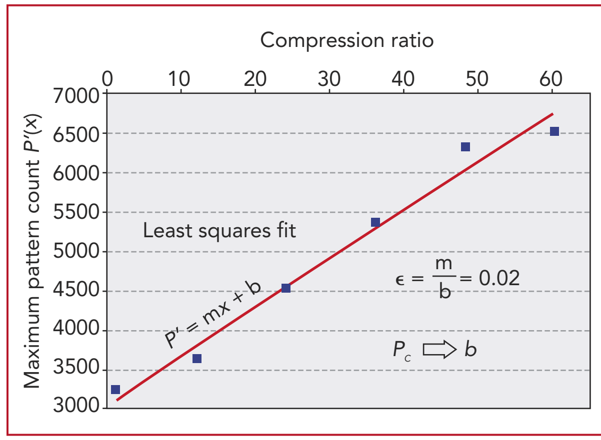

FIGURE 4. This graph plots pattern count vs. compression for an industrial design implemented at five different compression levels, where each point corresponds to the same fault coverage level. Once you calculate the least-squares curve fit, ϵ is just the ratio of the slope of the line to its y-intercept.

But the silicon-area-overhead cost places a limit on the full benefits of compression. For any design, an optimal compression level, λ, maximizes profits by minimizing test costs. The optimal compression level is unique for each product and is a function of process, design, DFT and compression architecture, tester configuration, and cost infrastructure. Table 1 summarizes how these parameters influence x_C and λ. You can use this table as a convenient guide on your way to discovering the most cost-effective compression strategy. T&MW

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Chris Allsup, *marketing manager for test automation products at Synopsys, has more than 20 years combined experience in IC design, field applications, sales, and marketing. He earned a BSEE degree from UC San Diego and an MBA degree from Santa Clara University.*

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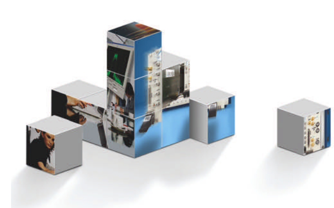

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MARTIN ROWE, SENIOR TECHNICAL EDITOR

Signal-integrity engineers measure and model connectors, cables, backplanes, ICs, and systems so designers can predict performance.

Signal-integrity measurements are essential to the development of high-speed communications systems. The higher a signal's frequency, the more susceptible it is to degradation. Digital signals, especially those over 1 Gbps, lose amplitude and accumulate jitter as they travel through connectors, printed-circuit board (PCB) traces, vias, IC pins, and cables (**Figure 1**). Thus, the transmission channels "offend" a signal's integrity.

Digital circuit designers often rely on signal-integrity (SI) labs and engineers to characterize their transmission systems and create HSPICE models that the designers can use to simulate the performance of an individual circuit or an entire system. With these models, designers can predict how a component will behave in both the time domain and the frequency domain.

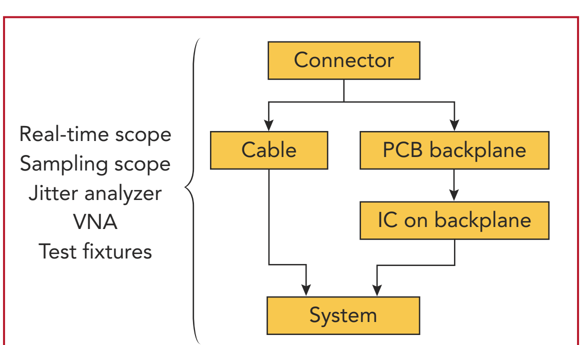


FIGURE 1. Connectors, cables, backplanes, and ICs contribute to signal losses in electronics systems.

Figure 2 shows a signal that degrades as it travels along a trace in a standard FR4 PCB. A serial data stream with a clean, wide eye diagram enters the trace, but after traveling 34 in., the signal is unrecognizable. Designers can compensate for the distortions that cause eyes to close by adding adaptive equalizers to their data receivers, but to do that, they need to know the condition of the eye.

Connectors and cables

Connector, cable, backplane, and component makers often test and model their products in the time domain using sampling and real-time oscilloscopes, bit-error-rate testers (BERTs), and time-domain reflectometers (TDRs). They may also make fre-

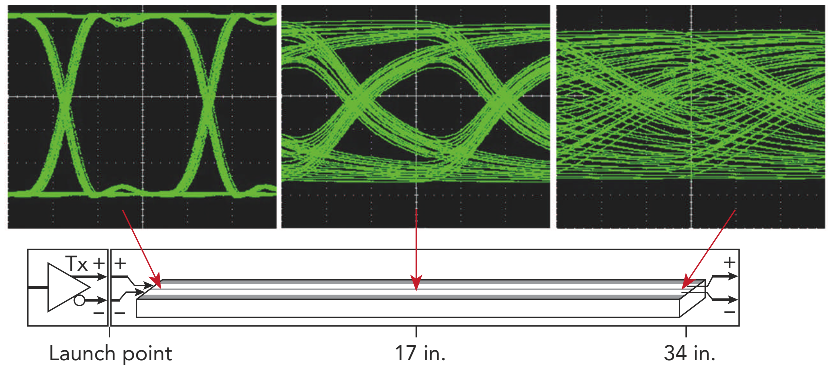


FIGURE 2. High-speed serial data streams lose amplitude and accumulate jitter as they travel through a PCB backplane. Courtesy of Tektronix.

quency-domain measurements using microwave test equipment such as spectrum analyzers and vector-network analyzers (VNAs).

"We test connectors at data rates up to 12 Gbps and at frequencies up to 20 GHz," said Dave Helster, director of circuit test and design at Tyco Electronics, a manufacturer of connectors used to carry both serial data streams and microwave signals. In the time domain, the company's engineers perform TDR measurements to determine a connector's impedance. In the frequency domain, the engineers produce S-parameter models of their connectors using VNAs.

At such high frequencies, test fixtures, probes, and cables offend and degrade signals. Tyco Electronics engineers must calibrate their test setups using standards and then mathematically compensate for the effects of the test setup to ensure they are measuring the S-parameters of the device under test (DUT). Once the engineers know how a test setup affects a signal in the frequency domain, they apply calibration factors to their measurements from which they produce a model of a DUT's characteristics such as frequency response.

At cable manufacturer W.L. Gore & Associates, SI engineers characterize microwave cables at frequencies to 110 GHz. They make S-parameter measurements on cables for digital signals at speeds up to 10 Gbps. "We test at data rates from 5 Gbps and higher," said technology development leader Tamera Yost. Gore's SI lab has equipment that can run at 12 Gbps.

Because many serial data streams use differential signals, each cable needs four-port S-parameter measurements. To make these four-port measurements with their two-port VNA, the lab's SI engineers designed a test box that uses microwave switches.

Although cables attenuate high frequencies more than they attenuate low frequencies, low-frequency measurements are still important because equalizers in serial-data receivers process signals differently depending on frequency. Thus, Gore's SI engineers use two VNAs to get a complete picture of a cable's characteristics. One VNA covers 30 kHz to 1 GHz, and another covers 1 GHz to 20 GHz.

To analyze the jitter that cables and connectors add to digital signals, Yost and her colleagues use a digital communication analyzer with jitter-analysis software. "Five or six years ago," noted Yost, "you just needed to measure total jitter (T_j) and separate it into deterministic jitter (D_j) and random jitter (R_j). It's not that simple anymore. Now, we have to measure data-dependent jitter (DD_j) based on bit patterns." DD_j measurements let engineers learn which communication protocols affect signal quality.

Boards and backplanes

SI engineers at Gore also study how PCB materials affect high-frequency signals. They see the effects of board thickness on signals. The thicker the PCB, the more vias become transmission-line stubs that degrade signals because they can radiate interference and cause signal reflections.

Engineers at Elma Bustronic see similar problems when they design backplanes. "Backplane thickness is now less than 4 mm because of stubs," said director of engineering Bagdan Gavril. Holes should be only as long as necessary, and the extra metal from a via that's too long acts like another piece of trace. "The extra capacitance [that the extra metal introduces] can kill a signal," Gavril noted.

Gavril asserts that at frequencies above 1 GHz, you have to pay attention to mistakes in board design that aren't important at lower frequencies. Above 3 GHz, every imperfection is critical. Elma's cus-

SI analysis capabilities vary

Andy Harkenson, product marketing manager at Wavecrest, a manufacturer of signal-integrity analyzers, sees three levels of SI capability at companies he visits: basic, intermediate, and advanced. The capabilities vary depending on company size and on whether the engineers need functional measurements, such as bit-error rate, or compliance measurements, such as jitter and timing.

Companies at the basic level don't have dedicated SI engineers. Instead, design and test engineers may perform some SI measurements. "I see engineers who are happy with just some basic jitter analysis," Harkenson said. At the intermediate level, a company starts to realize the importance of the SI function and may start performing TDR or frequency analysis.

Harkenson noted that advanced labs will have engineers dedicated to SI measurements and modeling who do no design work. These engineers also begin to understand how test equipment works and understand that equipment from different manufacturers can deliver different results, especially when it comes to jitter.—*Martin Rowe, Senior Technical Editor* tomers are currently specifying data rates of 6.25 Gbps, and Gavril expects inquiries for 10 Gbps before the end of 2007.

Elma Bustronic's SI engineers use VNAs to characterize transmission channels in backplanes. They measure impedance, make eye-diagram measurements, and measure backplane jitter. They also measure S-parameters and produce HSPICE models for their customers that incorporate data from connector and PCB models. Signal integrity is, therefore, a chain that moves up from connectors to boards to active components and then to systems.

Active components

No electronic system is complete without ICs such as field-programmable gate arrays (FPGAs), and at FPGA-manufacturer Xilinx, the SI engineers measure many of the same parameters as those at connector, cable, and backplane companies. The company's SI engineers characterize SerDes transmitters and receivers and provide HSPICE models that customers use in system designs. Jerry Chuang, manager for system I/O and SerDes devices, and his colleagues also study how PCB designs and board materials affect signals. But Xilinx customers design their own PCBs and thus must characterize their transmission channels based on information about Xilinx's products.

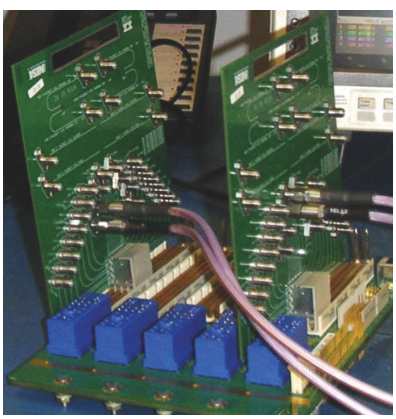


FIGURE 3. A test board for PCI Express connects directly to the backplane. Connectors provide access for test equipment. Courtesy of Elma Bustronic.

Xilinx engineers place extra emphasis on jitter. They must demonstrate to customers their devices' jitter performance because jitter is protocol specific. Protocols such as SONET, PCI Express, and XAUI produce different T_j, D_j, and R_j for any given data rate.

"We measure jitter with both sampling scopes and real-time scopes on serial-bus transmitters," said Chuang. "We need to understand how each scope manufacturer decomposes jitter because there is a difference." The Xilinx SI lab uses high-end real-time scopes with bandwidths that keep up with the data rates supported by the company's devices.

IC designers see problems that engineers at passive-component makers don't. ICs require power, and power supplies can affect signal integrity. "Signal integrity starts at DC," said Mark Marlett, principal design engineer at LSI Logic. He pointed this out because his company's ASICs can draw up to 7 A, and power supplies don't produce noise unless they're loaded. The company's SI engineers look at how noisy power supplies affect the quality of signals. Noise on a power supply, for example, can add jitter to clock signals. (For more on how Marlett and his team automate measurements, see "Test voices," p. 8.)

To evaluate the impact of power supplies, the engineers will look at a device in a powered but idle state with just the clocks running. Then, they activate portions of the ASIC, which increases current from the supply, and observe how the increased power-supply load affects jitter. They also investigate how backplanes, cables, and connectors affect signal quality.

SI in systems

Manufacturers of entire electronic systems need to be concerned about SI once connectors, backplanes, cables, and ICs come together to form a system. One such company is QLogic, a manufacturer of storage area networks. QLogic's SI lab consists of four engineers who measure S-parameters, rise time, jitter, intersymbol interference, noise level, and optical power. The engineers also test for receiver jitter tolerance. Data rates reach 8.5 Gbps for Fibre Channel systems.

QLogic principal engineer Douglas Zhao emphasized the importance of jitter measurements. "We measure T_j, R_j, DD_j, and sinusoidal jitter [$sine_j$] in transmitted data streams. We also test receiver jitter tolerance by adding jitter to clean data streams." The SI engineers also use a clean signal and reduce a signal's optical power to test receivers. They often release these test results to customers.

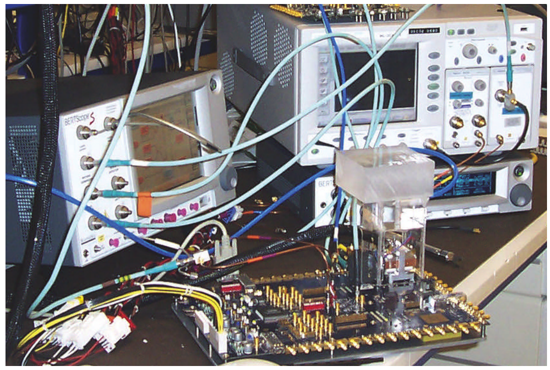


FIGURE 4. Engineers at LSI Logic use this test board to measure jitter and eye openings on signals moving to and from ASICs. Courtesy of LSI Logic.

The QLogic engineers also measure the noise in PCB power planes with a real-time scope and a spectrum analyzer. Spectral peaks often indicate resonances in components and PCBs that offend signal integrity.

Common ground

Regardless of whether they work on components or entire systems, SI engineers tend to make similar kinds of measurements and thus encounter similar obstacles. Perhaps the biggest challenge they face is finding a way to probe circuits and signals.

To simplify this task, engineers at many companies develop test boards and fixtures that make the signals accessible to test equipment. Of course, the SI engineers must calibrate the connection setup to compensate for the effects of the board or fixture itself on signal integrity.

Elma Bustronic, for example, uses a test board that gives engineers access to eight differential signal pairs through SMA connectors. The board also provides access to shorts and opens and has a MicroTCA edge connector that plugs directly into a backplane connector (**Figure 3**).

LSI Logic's Marlett uses the test board shown in **Figure 4**. His test setup enables him to measure jitter and eye openings on signals moving to and from ASICs.

SI engineers at Gore designed a test fixture that lets them test bulk cable. "It's a differential to coaxial transition," noted Yost. A differential cable has a 100-Ω impedance, but test equipment has a 50-Ω input impedance. The fixture lets SI engineers connect to bulk cable without having to add SMA connectors, which, like everything in a signal path, offend the signal of interest.

RF experience is becoming a necessity for SI engineers

Measurement experience helpful

What does it take to work as an SI engineer? Although there's no single answer to that question, RF experience is becoming a necessity, as digital signals take on analog characteristics. Company's that employ RF engineers have an advantage, because they can teach digital engineers on the ways of analog. A background in statistics can also be an advantage.

At QLogic, the SI engineers have different areas of expertise. One has system experience, another specializes in modeling, and a third specializes in test-equipment specifications and performance.

At large companies such as Gore, entire SI labs can have different specialties. The company's Elkton, MD, lab focuses on digital and microwave measurements, but its engineers in Germany have EMI expertise.

When asked what skills an SI engineer should have, Greg LeCheminant, measurement development engineer at Agilent Technologies, responded, "You need lots of measurement experience."

"Experience with frequency-domain analysis is also helpful," added Tyco's Helster, "but mostly, we look for highly motivated engineers who are willing to learn, because colleges don't teach about signal integrity." T&MW

FOR FURTHER INFORMATION

Rowe, Martin, "Jitter discrepancies: not explained," a sidebar in "The scopes trial," by Dan Strassberg, *EDN*, February 6, 2003. www.edn.com.

"Setting up a Signal Integrity Lab," Wavecrest, Eden Prairie, MN. www.wavecrest.com.

Grandmaster clock keeps precise time

Symmetricom's XLi Grandmaster clock synchronizes network nodes and measures a network's latency. Getting time through its GPS receiver, the XLi can synchronize thousands of IEEE 1588-compliant network nodes with its time-stamp processor and produce time stamps accurate to within 50 ns of Coordinated Universal Time (UTC).

The XLi uses IEEE 1588 to measure latency between itself and a slave by comparing its 1-pulse-per-second (pps) output to that of the slave, and it is accurate to 5 ns. The XLi can also perform statistical analysis of the time intervals revealed by the slave's mean clock offset from the Grandmaster and the distribution around the mean.

The XLi Grandmaster Clock is available with one or two IEEE 1588 ports. You can configure the second port as a master or slave. The clock also contains an alarm output and an input for IRIG-A, IRIG-B, or NASA-36 codes.

Prices: XLi with one 1588 port—$9,995; with two 1588 ports—$12,495. *Symmetricom, www.symmttm.com.*

Agilent debuts DigRF logic-analyzer probes

The N4850A digital-acquisition probe and the N4860A digital-stimulus probe support cross-domain measurements for the design, validation, and integration of 2.5G and 3G baseband and RF ICs that comply with the DigRF v3 standard, which defines a 312-Mbps serial digital interface between RF and baseband ICs in cell phones.

The new probes work with an Agilent 16800 or 16900 logic analyzer. The acquisition probe requires a 68-channel (minimum) instrument and comes with differential flying leads that permit probing close to the signal source while maintaining signal integrity. The stimulus probe supports SMA cables as well as flying leads.

Using the tools, handset integration teams can evaluate product behavior by monitoring the digital serial bit stream between an RF IC and a baseband IC. Adding Agilent's 89601A digital vector-signal-analysis package to the logic analyzer provides the ability to perform digital I/Q analysis.

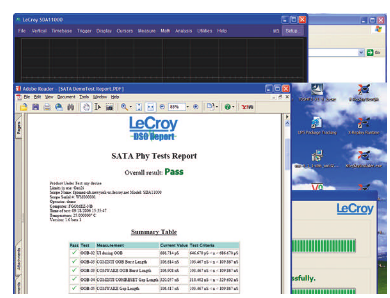
In addition, RF IC development teams can evaluate their components independent of the baseband IC. For transmitter evaluation, designers can create signals using Agilent's Signal Studio software and load them into the logic analyzer to stimulate the RF chip's DigRF v3 interface. Designers can capture the resulting RF signal with an N9020A signal analyzer.

For receiver evaluation, an E4438C ESG vector signal generator can stimulate the RF IC. The digital-acquisition probe can acquire the digital I/Q that the RF IC generates for subsequent vector signal analysis.

Baseband IC designers can also use the tools to evaluate their chips independent of an RF chip. Validation teams can use the N4850A acquisition probe to analyze transmitted DigRF v3 control and data traffic. A protocol view of control traffic and vector signal analysis of data traffic enable cross-domain debug. With the addition of the Agilent N4860A stimulus probe, the receive path on the baseband IC can be exercised.

Base price: $14,495 for each probe. *Agilent Technologies, www.agilent.com.*

Automate physical-layer compliance tests



Products that use a serial data bus require physical layer (PHY) compliance testing to an industry standard. Often, the standard specifies waveform shapes and eye-diagram limits that you view on an oscilloscope. LeCroy's QualiPHY accessory lets you automate PHY testing on Ultra Wideband (UWB), SerialATA (SATA), Ethernet, USB, and fully buffered DIMM (FB-DIMM) serial buses.

QualiPHY includes software and a test fixture that lets you make all oscilloscope measurements required by a standard. The software operates with all LeCroy scopes that have 2-GHz or higher bandwidth. You can run the QualiPHY software either directly in the scope or on a remote PC connected to the scope by IEEE 488 or Ethernet. The software controls the scope, collects the data, and produces test reports in HTML, RTF, PDF, or XML format.

Prices: UWB—$6995, SATA—$4995, FB-DIMM—$4995, Ethernet—$2995, USB—$2995. *LeCroy, www.lecroy.com.*

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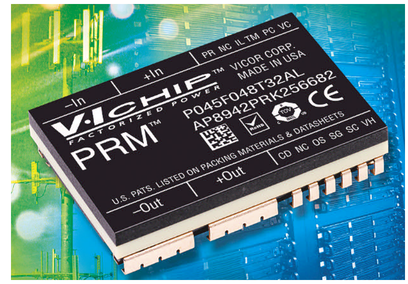
Vicor introduces 320-W regulator

Vicor has introduced a high-power-density (greater than 1100 W/in3) 320-W PRM (pre-regulator module) non-isolated regulator. Designated P045F048T32AL, this latest component in the vendor's VI Chip family is designed for 48-V power applications involving automated test equipment, servers, and telecom equipment.

This PRM provides a controlled distribution voltage for powering downstream VTM (voltage transformation module) current multipliers, creating fast, efficient, isolated, low-noise point-of-load (POL) converters.



With an efficiency of 97% and matched with a 94% efficient VTM unit, it enables direct 48-V-to-load with 91% efficiency, eliminating the need for an intermediate 12-V bus-conversion stage and VRMs.

In combination, PRMs and VTMs form a complete DC-DC converter subsystem based on Vicor's Factorized Power Architecture (FPA), which offers high density and efficiency, low-noise operation, architectural flexibility, fast transient response, and elimination of bulk capacitance at the point of load. A PRM+VTM chip set provides up to 100 A or 300 W for a 48-V direct-to-load density of over 500 W/in^3. Alternatively, the PRM may be used independently if isolation is not required.

The P045F048T32AL features adaptive-loop compensation feedback. This single-wire alternative to traditional remote sensing and feedback loops enables precise control of an isolated POL voltage without the need for either a direct connection to the load or for noise-sensitive, bandwidth-limiting, isolation devices in the feedback path.

Base price: $53 (OEM quantities) for a 320-W PRM+VTM chip set to convert from 48 V direct to 1 V. *Vicor, www.vicr.com.*

Stand-alone controller runs Linux

United Electronic Industries has introduced the UEIPAC line of programmable automation controllers. These stand-alone PAC modules contain an embedded computer running a standard Linux operating system, two Ethernet ports, a serial port, a Secure Digital (SD) card interface, an inter-PAC sync interface, and either three or six I/O card slots.

I/O boards add up to 150 analog inputs and 288 digital I/O channels. Other I/O boards add analog outputs, counter/timer channels, quadrature encoders, serial ports, CAN bus ports, and ARINC-429 interfaces. You can write your application on a PC and download it to the controller, which can then operate as a stand-alone unit. The modules operate in harsh environments from –40°C to +85°C, at 5-g vibration, at 50-g shock, and at up to 70,000 ft in altitude for aerospace testing.

Prices: UEIPAC 300 (3 I/O board slots)—$1495; UEIPAC 600 (6 I/O board slots)—$1795. *United Electronic Industries, www.ueidaq.com.*

Anritsu enhances broadband VNA

Anritsu has enhanced its Lightning Broadband ME7808C vector network analyzer (VNA), which characterizes devices over a wide 40-MHz to 110-GHz frequency range. The VNA has been redesigned to provide higher output power to drive active and passive components at optimum measurement levels, and it features improved calibration stability.

Engineers can use the ME7808C in coaxial or on-wafer environments. Among the design enhancements are the relocation of couplers inside the instrument's multiplex combiners, improved Kelvin design bias tees, better RF and LO stability, and greater short-term and long-term calibration and measurement stability. The system now includes an option providing direct sampler access for improved raw directivity and to optimize calibration while optimizing system dynamic range.

The new multiplexing coupler/combiner allows all essential DC signals and RF sampling to be in close proximity to the device under test (DUT), further improving raw directivity as well as increasing measurement system stability. Designed into the multiplexing modules are the Kelvin bias tees for enhanced performance and sensitivity. The ME7808C has also been designed with improved phase-stable cables for better calibration and measurement stability.

The ME7808C can provide up to –13 dBm of power across the entire 40-MHz to 110-GHz frequency range, which, Anritsu says, is 9-dB better than competitive models. Power output is a significant factor in measurement accuracy because losses between the coax output port and the probe tips can be dramatic.

The ME7808C can be configured for three configurations: a 40-MHz to 110-GHz 1-mm broadband coaxial system; a 65-GHz V-connector coaxial system; and a 65-GHz to 110-GHz extended W-band waveguide mm-wave system. The system may be upgraded to include a range of banded mm-wave modules, which can be used to extend the frequency range beyond 110 GHz in stand-alone waveguide bands. In addition, it is now possible to extend the maximum waveguide frequency range up to 500 GHz in a WR-2.2 waveguide.

Base price: $384,455. *Anritsu, www.us.anritsu.com.*

Power supplies offer soft-panel interfaces

Chroma's 62000P series of DC power sources and the 66200 power meter now include graphical soft panels that allow users to control instruments remotely using point-and-click screens on any Windows-based PC. Once installed, the soft panel communicates with the instrument through an RS-232 or GPIB interface.

The soft panel for the DC power source enables users to program test sequences, square waves, triangle waves, and other voltage ramp functions, as well as control multiple sources in parallel, series, or independently.

The power meter's soft panel helps users control voltage and current readings and ranges, frequency readings, THD measurements, user-defined criteria for pass/fail information, real-time measurements, report generation, in-rush current and energy measurements, and real-time GUI graphing.

Chroma System Solutions, www.chromausa.com.

Spectrum analyzer includes Tablet PC

The BumbleBee-Tablet from Berkeley Varitronics combines a spectrum analyzer with a Windows XP Tablet-based Ultra-Mobile PC. The portable instrument allows users to measure a variety of wireless bands for network installation, coverage, and RF interference analysis.

BumbleBee-Tablet's calibrated receiver supports WiFi, WiMax, ISM, and Bluetooth. It features a 7-in. WVGA LCD

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touchscreen and a Pentium processor, as well as an internal 40-Gbyte hard drive for storage and playback of RF spectral-analysis data.

Other features include power triggers, three pairs of markers, histograms, video smoothing, waveform averaging, one live trace, and up to four peak-hold waveform traces with peak hold and peak search. Optional interference mapping software and direction-finding antenna kits are available.

Berkeley Varitronics Systems, www.bvsystems.com.

Acquisition recorder works in airborne installations

Designed for a wide range of operational and flight-test applications, the D7000 data-acquisition and recording system from the Heim Data division of Zodiac Data Systems acquires data from multiple avionics signal sources and records it to interchangeable media cartridges. The D7000 also provides adaptable signal interfacing in a rugged, compact package built for harsh environments.

With up to a 256-Mbps total system data rate, the system employs a packet recording format that ensures accurate data time tagging and consistent channel-to-channel phase relationships. The D7000 is compatible with both the Heim Data format and the IRIG106 Chapter 10 standard.

The mainframe also has GigE data download capability, and the media SCSI interface provides a high-speed output to other Heim Data systems. Its internal IRIG time code generator lets you synchronize to external IRIG and GPS time sources. In addition, the unit can optionally be fitted with an internal GPS receiver.

The mainframe holds up to four multichannel signal-interface cards, enabling concurrent recording of multiple video, PCM, and MIL-STD-1553 bus sources.

Heim Data, Zodiac Data Systems, www.zds-us.com.

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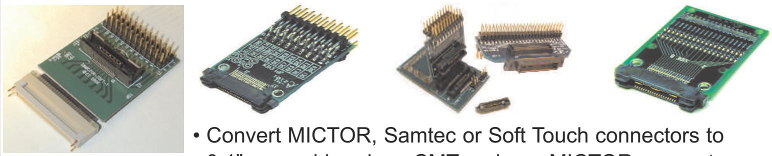

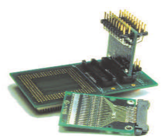

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[An exclusive interview with a technical leader]

BRAD BYRUM
General Manager
Test & Measurement Division
Yokogawa Corp. of America
Newnan, GA

Brad Byrum has more than 18 years of experience in the test equipment industry as a test engineer, application engineer, product manager, marketing manager, and business unit manager. At Yokogawa, Byrum is responsible for all marketing, product management and business operations in North America for the Test and Measurement Division. He holds a BS degree in electronic engineering technology.

Contributing editor Larry Maloney spoke with Byrum about industry trends in a recent telephone interview.

Helping engineers do more with less

Q: What is Yokogawa's niche among test field vendors?

A: Yokogawa positions itself as a technology leader. The company invests about a quarter billion dollars a year on research and development, much of it aimed at core technologies like test and measurement. Since 1915, we've amassed more than 6000 patents. A lot of that effort is going into developing key technologies, such as 40-Gbit components, analog-to-digital converters, sensors, MEMs, and networking technologies. This research eventually filters down into next-generation products.

Q: Can you give an example of an important new product that embodies what Yokogawa strives to do with its technology?

A: A good example is the DL9000 signalXplorer series of digital oscilloscopes, which last year won a Best in Test award from your magazine. It boasts an acquisition rate of up to 2.5 million frames/s/channel. So, the data engine inside of it is enormously fast. But because we developed this instrument internally, we can offer this high-performance product at a very attractive price (starting around $11,000). Our idea was to introduce a 1-GHz scope at a 500-MHz price. After the initial rollout, we also have been adding more and more capability to the product, such as power analysis, controller area network (CAN) bus analysis, and real-time analysis of Inter-IC and Serial Peripheral Interface buses.

Q: What is the potential for your testers in automotive FlexRay applications?

A: The FlexRay in-vehicle control network, which can transmit and receive data 10 times faster than a conventional CAN, is expected to come into wide use in the coming years. Yokogawa has been a member of the FlexRay Consortium, formed in 2000 to develop standards for this new network. In the test arena for FlexRay, engineers initially are looking for physical layer analysis to work out the hardware bugs, and we are providing the DL7400 FlexRay analyzer for that work. As engineers work past the hardware bugs, they begin to look at interconnect issues, such as chipset to chipset, and they need to generate FlexRay data for protocol analysis. At last fall's Auto Test Expo, we previewed a new data generator and protocol analyzer for that task. FlexRay is clearly a growth area that we are committed to support.

Q: How about other promising opportunities in automotive?

A: Higher energy costs have really pushed development of new hybrid vehicle design, and we expect that area to be very active over the next decade. Our AC power analyzers are very popular with engineers working in hybrid vehicles. They want to measure the efficiency of their drive train designs, which means analyzing the battery power source, the bus, the inverter, the motor, and the mechanical output power. Our power analyzers can show the efficiency of each phase of this drive train, as well as the total efficiency of the system.

Q: What do you see as the biggest challenges that test engineers face on the job?

A: You can sum it up with the phrase "doing more with less." Engineers are constantly being tasked with covering not only their core competencies but also areas that fall outside that core expertise. So, a software engineer suddenly is asked to take on a hardware project, or a semiconductor FPGA guy gets a power-supply design job. This in turn drives engineers to depend on test equipment manufacturers to make tools that fill these gaps and make testing easier and more intuitive. T&MW

Brad Byrum gives additional comments on test applications for fuel cells, optical communications, and mobile phones in the online version of this interview: www.tmworld.com/2007_03.

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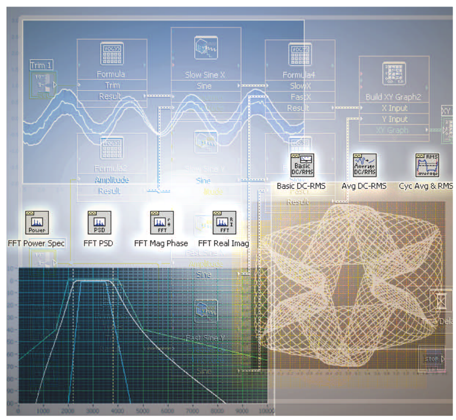

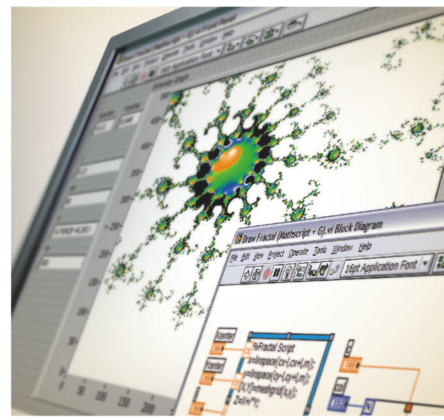

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